EK-AI7931HD
User Guide

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Document History

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1.Introduction

1.1.General Description

AI7931HD is a highly integrated stamp module that features an ARM® Cortex-M33 application processor, a low power 1x1 802.11a/b/g/n/ax dual-band Wi-Fi subsystem, a Bluetooth v5.0 subsystem and a Power Management Unit (PMU). The Wi-Fi subsystem and a Bluetooth v5.0 subsystem offer feature-rich wireless connectivity at high standards, and deliver reliable, cost-effective throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption.

AI7931HD is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance. The AI7931HD is based on ARM® Cortex-M33 with floating point microcontroller (MCU) including SRAM/ROM memory. The chip also supports rich peripheral interfaces, including UART, SDIO, I2C, SPI, I2S, and auxiliary ADC. These features are used to download and debug a project on EK-AI7931HD.

The front view of the EK-AI7931HD including AI7931HD stamp module and a FTDI debug board is shown in Figure 1.

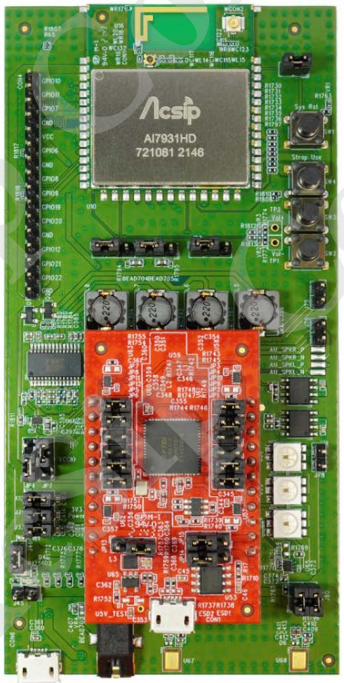

Figure 1. Front view of EK-AI7931HD and FTDI debug board

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2. Get started with the HDK

Before commencing the application development, you need to configure the development platform.

2.1. Configuring the EK-AI7931HD

EK-AI7931HD includes a Base Board, a AI7931HD stamp module and a FTDI Debug board. The top view of the EK-AI7931HD is shown in Figure 2

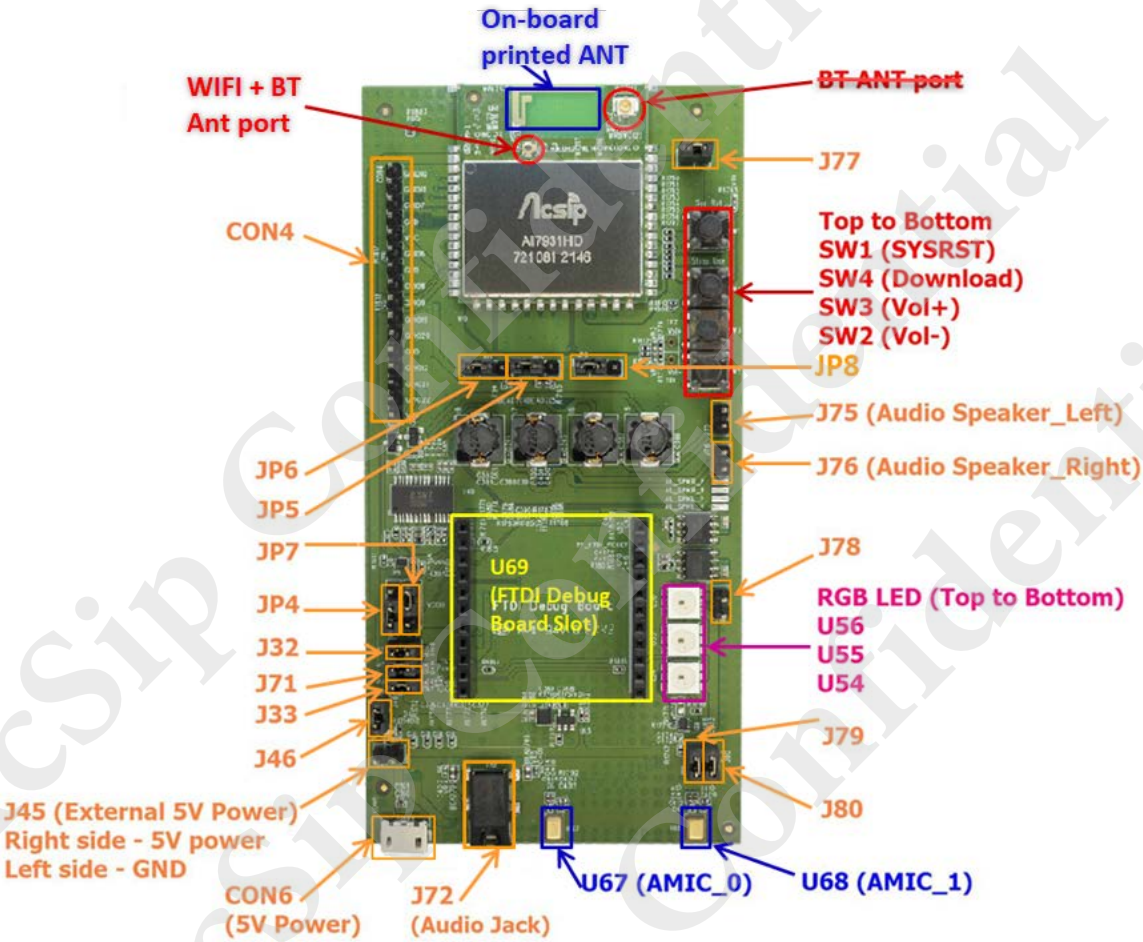

Figure 2. Jumpers and connectors on the EK-AI7931HD

The description of pins (Figure 2) and their functionality is provided below:

1) CON6 is a USB 5V power for AI7931HD stamp module, or you can use external 5V power at J45.
2) Press SW1 to reset the system For SW2~SW4 more detail, please see “section 4.4”.
3) For Wi-Fi and BT function AI7931HD stamp module reserve a Wi-Fi + BT RF-coaxial connector (MM8030-2610) and you can also use the on-board printed antenna to transmit and receive RF signal.

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4) The FTDI debug board can transfer USB interface to UART interface. Using this debug board can debug through UART, transmit, and receive a signal form PC.

5) U67 and U68 are on-board AMICs which can catch voice command.

6) J75 and J76 are audio speaker connectors which can connect 8ohm/2W speaker to achieve voice assistant function.

7) U54/U55/U56 are RGB LEDs and these RGB LED will be controlled by SPIM interface.

8) CON4 support multifunction GPIO interface, for more detail please refer to “section 4.7”.

2.2.Installing the FTDI debug board drivers on Microsoft Windows

To configure the EK-AI7931HD:

1) Ensure the FTDI debug board insert to EK-AI7931HD at U69.

2) Connect the FTDI debug board to the computer using a micro-USB cable.

3) Connect a 5V power at EK-AI7931HD CON6 with a micro-USB cable.

4) Check your PC is X86 or X64 system and download and install FTDI Windows serial port driver from Here (The red block showed the download file at below figure).

Currently Supported D2XX Drivers:

		Processor Architecture					
Operating System	Release Date	x86 (32-bit)	x64 (64-bit)	ARM	MIPS	SH4	Comments
Windows*	2017-08-30	2.12.28	2.12.28	-	-	-	WHQL Certified. Includes VCP and D2XX. Available as a setup executable Please read the Release Notes and Installation Guides.
Windows RT	2014-07-04	1.0.2	-	1.0.2	-	-	A guide to support the driver (AN_271) is available here
Linux	2018-06-22	1.4.8	1.4.8	1.4.8 ARMv5 soft-float 1.4.8 ARMv5 soft-float uClibc 1.4.8 ARMv6 hard-float *** 1.4.8 ARMv7 hard-float *** 1.4.8 ARMv8 hard-float ***	1.4.8 MIPS32 soft-float 1.4.8 MIPS32 hard-float 1.4.8 MIPS openwrt-uclibc		If unsure which ARM version to use, compare the output of `readelf` and `file` commands on a system binary with the content of release/build/libftd2xx.txt in each package. ReadMe NEW! Video Install Guide

5) If your OS is Windows7 or 10, please open Windows Control Panel then click System and enter Device Manager.

6) In Device Manager, navigate to Ports (COM & LPT) (see Figure 3).

7) A new COM device should appear under Ports (COM & LPT) in Device Manager, as shown in Figure 3. Note the COMx port number of the serial communication port, this information is needed to send command and receive logs from the COM port.

Due to the com port numbers (COMx) are different at different PC. In order to check the function of each com port we can recognize the order of these com ports as Figure 3 showed, the first com port (#1) means “DSP UART”, the second com port (#2) mean “UART0”, the third com port (#3) mean “UART1”, the fourth com port (#4) mean “CM33 UART”.

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Figure 3. COM port associated with the EK-AI7931HD

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3.Hardware Features

This section provides the main supported features of the EK-AI7931HD The detailed description of the features is provided in the upcoming sections

3.1.Features Description

3.1.1. Technology and Package

- AI7931HD Stamp Module: 30mm X 34mm X 2.7mm

3.1.2. Power Management and Clock Source

- Integrates high efficiency power management unit with single 3.3V power supply input.
- Integrates 26MHz crystal clock with low power operation in idle mode.
- Integrates 32KHz crystal oscillator for low power sleep mode.

3.1.3. Platform

- ARM® Cortex-M33 MCU with FPU with up to 300MHz clock speed.
- Embedded 1MB SRAM.
- Embedded 16MB serial flash with eXecute In Place (XIP) and on-the-fly AES.
- Supports Hardware crypto engines including AES, DES/3DES, SHA, ECC, TRNG for network security.
- Supports up to 22 General Purpose IOs, which are multiplexed with SPI, I2C, Aux ADC, UART, and GPIO interfaces.
- Supports 12 DMA channels.

3.1.4. Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ax 5GHz and 2.4GHz.
- Supports 20MHz, bandwidth in 2.4G/5GHz band, and MCS0~MCS8.
- Support uplink MU-OFDMA TX and downlink MU-OFDMA RX.
- Support STBC Rx, LDPC Tx, and RX Beamforming.
- Wi-Fi security WFA WPA/WPA2/WPA3 personal.
- Support 11ax TWT low power.
- Integrated balun, PA, LNA, and T/R switch.
- Support antenna diversity.

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3.1.5. **Bluetooth**

- Bluetooth v5.0 with 2Mbps PHY rate, Long-range and LE Advertising Extensions
- Integrated balun and PA.
- Supports BT/Wi-Fi coexistence.

3.1.6. **Miscellaneous**

- Embedded eFuse to store specific device information and RF calibration data.
- Advanced TDD mode Wi-Fi/Bluetooth coexistence scheme.

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4.Hardware Feature Configuration

4.1.Microcontroller

The MCU subsystem consists of a 32-bit MCU, the AHB/APB bus matrix, internal RAM/ROM with ROM patch function, the flash controller and the system peripherals including Direct Memory Access (DMA) engine and the General-Purpose Timer (GPT). The AI7931HD features an ARM® Cortex-M33 processor, which is the most energy efficient ARM® processor currently available. It supports the clock rates up to 200MHz when core power is 0.7V and 300MHz when core power is 0.8V.

The MCU executes the Thump-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication and bit-field manipulation. The AI7931HD includes a Memory Protection Unit (MPU) in Cortex-M33 MCU to detect unexpected memory access and provides other memory protection features. The AI7931HD also includes FPU in Cortex-M33 MCU.

4.2.Power supply

Power up with a micro-USB connector. An on-board switching regulator provides voltage of 3.3V for the EK-AI7931HD based on AI7931HD, if the power is supplied from an on-board micro-USB connector CON6 (Figure 2) Note, that the jumpers J46, J33, J32, JP4 pin2 and pin3 and JP7 pin2 and pin3 are required to be set on More details on the jumpers can be found in Table 1.

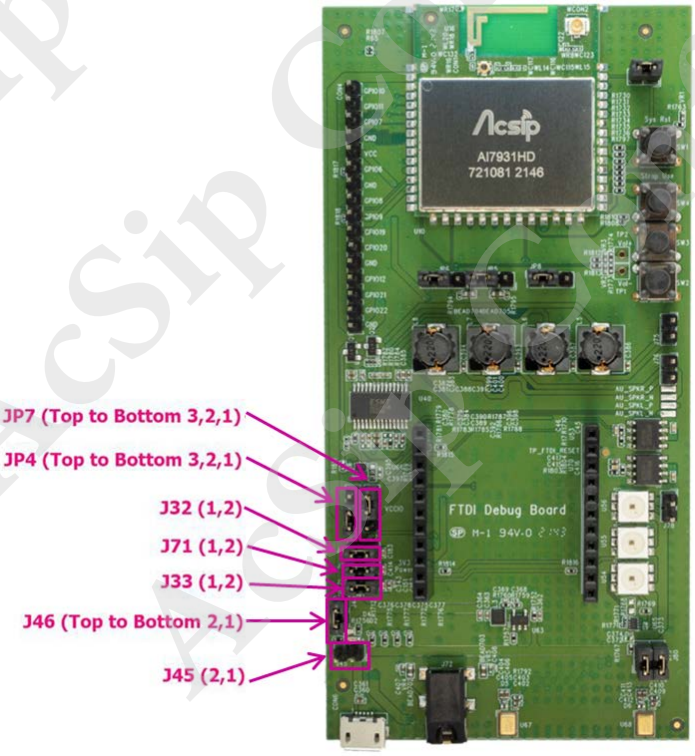

Figure 4. Default power jumper plot

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Table 1 Jumper settings for system power input through USB connection

Jumper	Usage	Comments
J45	External 5V power supply.	Use external power source to supply 5V voltage to AI7931HD. Pin 1 is 5V source, Pin2 is GND.
J46	3V3 for AI7931HD.	
J33	3V3 for external components.	
J71	Reserve for extra 3V3 request for other components.	
J32	3V3 for external LDO (1.8V and 0.8V)	
JP4	Switch VCCIO to 3V3 power domain	Select pin 1 & 2, means VCCIO use 3V3 power domain.
JP7	Switch 1V8 VCCIO from internal PHYLDOor external LDO.	Select pin 1 & 2, means 1V8 VCCIO from external buck component.

4.3. Audio

The EK-AI7931HD has on-board audio connector associated with different functionalities of the board. The detail of audio related function can refer to Table 2.

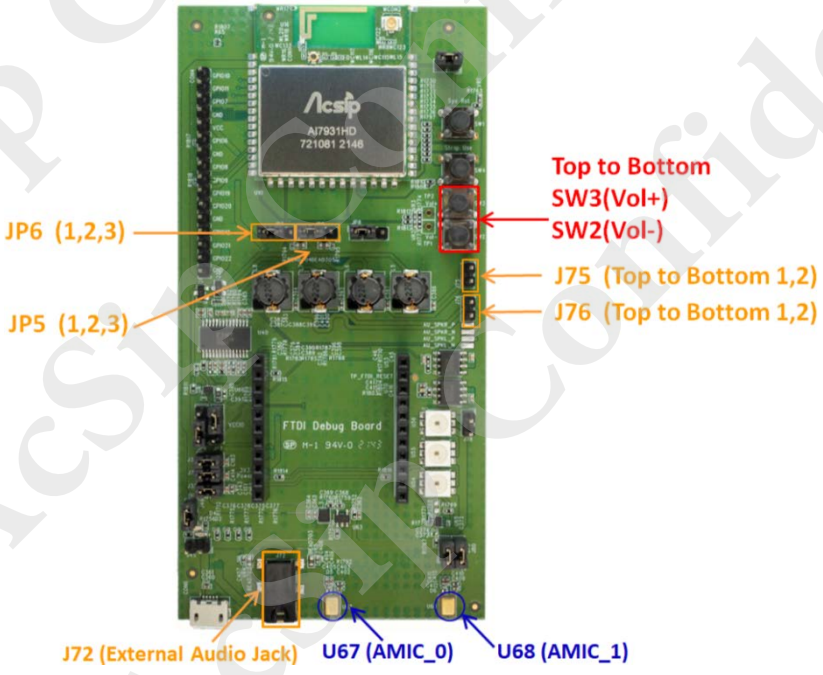

Figure 5. Audio related function

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Table 2 Audio related function

item	Detail
J72	3.5mm audio jack for external active speaker
J75	Audio header for left speaker
J76	Audio header for right speaker
U67	AMIC for left channel (the microphone hole is set at back side of EK-AI7931HD)
U68	AMIC for right channel (the microphone hole is set at back side of EK-AI7931HD)
SW3	Audio volume up button
SW2	Audio volume down button
JP5	This jumper switches the audio output trace: Select to pin1 and pin2 means audio output to audio jack Select to pin2 and pin3 means audio output to J75
JP6	This jumper switches the audio output trace: Select to pin1 and pin2 means audio output to J76 Select to pin2 and pin3 means audio output to audio jack

4.4.Buttons

The EK-AI7931HD is equipped with buttons with the following functionality.

The push buttons are shown in Figure 2 The detail of buttons can refer to Table 3.

Table 3 Buttons

Button	Name	Detail
SW1	SYSRST	Press SW1 to restart the EK-AI7931HD
SW2	Vol-	Audio volume down button
SW3	Vol+	Audio volume up button
SW4	Download key	Press SW4 to make EK-AI7931HD strap into download mode

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4.5.Antenna

By default, the board ships with RF signals routed to the on-board printed antenna. And AI7931HD reserve a conductive test component, (RF-coaxial connector, MM8030-2610) enables to test the signals using a compatible cable. Please refer to Figure 6 to see more detail.

Figure 6. On-board printed antenna

4.6.RGB LED

As Figure7 showed, the EK-AI7931HD has on-board RGB LEDs (U54/U55/U56) which be controlled by SPIM interface. Please note that ensure jumper J79 and J80 are connected before using RGB LED function If you want to cascade more RGB LED, you can connect to J78

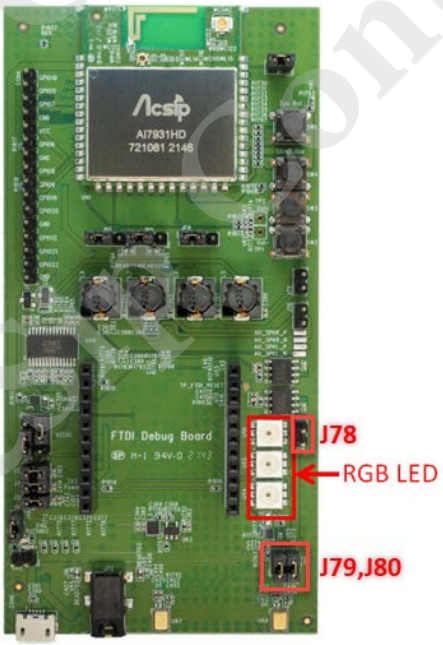

Figure 7. RGB LED

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4.7.Extension connectors

The EK-AI7931HD provides similar pin-out extension connectors for various sensor and device connectivity, as shown in Figure 8 and described in Table 4.

The board has 13 GPIOs multiplexed with other interfaces. Depending on the use case, user can configure each I/O functionality.

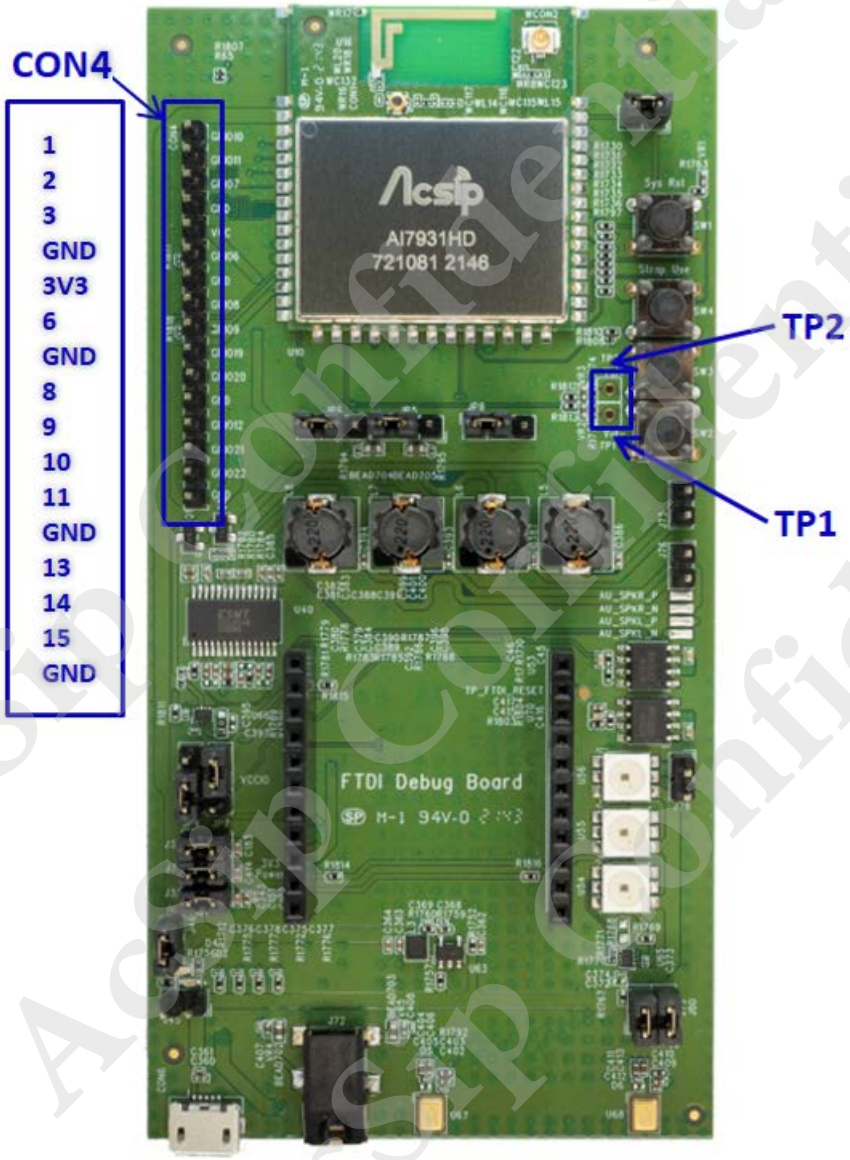

Figure 8. GPIO pin-out extension connectors

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Table 4 GPIO pin-out extension connector

Signa Name	Connector Pin Number	Signal Name	Connector Pin Number
GPIO_0	Reserve for flash	GPIO_15	TP2
GPIO_1	Reserve for flash	GPIO_16	TP1
GPIO_2	Reserve for flash	GPIO_17	Reserve for UART0
GPIO_3	Reserve for flash	GPIO_18	Reserve for UART0
GPIO_4	Reserve for flash	GPIO_19	CON4 – 10
GPIO_5	Reserve for flash	GPIO_20	CON4 – 11
GPIO_6	CON4 – 6	GPIO_21	CON4 – 14
GPIO_7	CON4 – 3	GPIO_22	CON4 – 15
GPIO_8	CON4 – 8	GPIO_23	Reserve for DSP UART
GPIO_9	CON4 – 9	GPIO_24	Reserve for DSP UART
GPIO_10	CON4 – 1	GPIO_42	Reserve for UART1
GPIO_11	CON4 – 2	GPIO_44	Reserve for UART1
GPIO_12	CON4 – 13	GPIO_48	Reserve for CM33 UART
GPIO_13	Reserve for ANT switch	GPIO_50	Reserve for CM33 UART
GPIO_14	Reserve for audio mute		

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Table 5 GPIO pin multi-function definition

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
PAD_SYSRST_B	NA	PAD_SYSRST_B			PU	Chip hardware fundamental reset pin
SDIO_CLK	0000	GPIO[6]	I/O	I	PD	GPIO 6
	0001 *	SDIO_CLK	I			SDIO Clock
	0010	MSDC0_CLK	O			MSDC Clock
	0011	SPIM0_SCK	O			SPI0 (Master) Clock
	0100	CM33_GPIO_EINT0	I			CA33 EINT0
	0101	DEBUG_0	O			Debug signal
	0110	ANT_SEL0	O			Antenna Select 0
	0111	BGF_EINT_10_B	I			
SDIO_CMD	0000	GPIO[7]	I/O	I	PU	GPIO 7
	0001 *	SDIO_CMD	I/O			SDIO Command
	0010	MSDC0_CMD	I/O			
	0011	SPIM0_CS_N	O			SPI0 (Master) Chip Select
	0100	CM33_GPIO_EINT1	I			CA33 EINT1
	0101	DEBUG_1	O			Debug signal
	0110	ANT_SEL1	O			Antenna Select 1
	0111	PINMUX_EXT_INT_N	I			
SDIO_DAT0	0000	GPIO[8]	I/O	I	PU	GPIO 8
	0001 *	SDIO_DAT0	O			SDIO Data[0]
	0010	MSDC0_DAT0	I/O			MSDC0 data0
	0011	SPIM0_MISO	I			SPI0 (Master) Input
	0100	UART0_RTS	O			
	0101	DEBUG_2	O			Debug signal
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CA33 EINT0
SDIO_DAT1	0000	GPIO[9]	I/O	I	PU	GPIO 9
	0001 *	SDIO_DAT1	I/O			SDIO Data[1]
	0010	MSDC0_DAT1	I/O			MSDC0 data1
	0011	SPIM0_MOSI	O			SPI0 (Master) Output
	0100	UART0_CTS	I			UART0 Control
	0101	DEBUG_3	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CA33 EINT1

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IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
SDIO_DAT2	0000	GPIO[10]	I/O	I	PU	GPIO 10
	0001 *	SDIO_DAT2	I/O			SDIO Data[2]
	0010	MSDC0_DAT2	I/O			MSDC0 data2
	0011	I2SIN_DAT0	I			
	0100	UART0_RX	I			UART0 RX
	0101	DEBUG_4	O			Debug signal
	0110	I2C0_SCL	I/O			
	0111	CM33_GPIO_EINT2	I			CA33 EINT2
SDIO_DAT3	0000	GPIO[11]	I/O	I	PU	GPIO 11
	0001 *	SDIO_DAT3	I/O			SDIO Data[3]
	0010	MSDC0_DAT3	I/O			
	0011	I2SO_DAT0	O			I2SO Data
	0100	UART0_TX	O			UART0 TX
	0101	DEBUG_5	O			Debug signal
	0110	I2C0_SDA	I			I2C0 Data
	0111	CM33_GPIO_EINT3	I			CA33 EINT3
GPIO_B_0	0000	GPIO[12]	I/O	O	PU	GPIO 12
	0001 *	CONN_BGF_UART0_	O			
	0010	MSDC0_RST	O			MSDC0 reset
	0011	CONN_BT_TXD	O			
	0100	WIFI_TXD	O			
	0101	DEBUG_6	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT4	I			CA33 EINT4
GPIO_B_1	0000	GPIO[13]	I/O	I	PU	GPIO 13
	0001 *	USB_IDDIG	I			USB OTG ID pin
	0010	SPIM1_SCK	O			SPIM1 (Master) Clock
	0011	I2SO_BCK	O			I2SO BCK
	0100	UART1_RX	I			UART1 RX
	0101	DEBUG_7	O			
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT5	I			CA33 EINT5
GPIO_B_2	0000	GPIO[14]	I/O	O	PD	GPIO 14
	0001 *	USB_DRV_VBUS	O			USB OTG host mode
	0010	SPIM1_MOSI	O			SPI1 (Master) Output
	0011	I2SO_LRCK	O			I2SO LRCK
	0100					
	0101	DEBUG_8	O			Debug signal
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT6	I			CA33 EINT6
GPIO_B_3	0000	GPIO[15]	I/O	I	PD	GPIO 15
	0001 *	USB_OC	I			USB Host mode over-
	0010	SPIM1_MISO	I			SPI1 (Master) Input
	0011	I2SO_MCK	O			I2STX MCLK
	0100	I2SIN_MCK	O			I2SRX MCK
	0101	DEBUG_9	O			Debug signal
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT7	I			CA33 EINT7
GPIO_B_4	0000	GPIO[16]	I/O	I	PD	GPIO 16
	0001 *	USB_VBUS_VALID	I			USB device mode VBUS
	0010	SPIM1_CS_N	O			SPI1 (Master) Chip
	0011	IR_IN	I			
	0100	I2SIN_MCK	O			I2SRX MCLK
	0101	DEBUG_10	O			Debug signal
	0110	ANT_SEL7	O			Antenna Select 7
	0111	CM33_GPIO_EINT8	I			CA33 EINT8

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IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_5	0000	GPIO[17]	I/O	I	PU	GPIO 17
	0001 *	CONN_BGF_UART0_RXD	I			
	0010	UART0_RX	I			UART0 RX
	0011	TDMIN_MCLK	I			
	0100	DMIC_CLK0	O			DMIC CLK0
	0101	DEBUG_11	O			Debug signal
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT9	I			CA33 EINT9
GPIO_B_6	0000	GPIO[18]	I/O	O	PU	GPIO 18
	0001 *	CONN_BT_TXD	O			
	0010	UART0_TX	O			UART0 TX
	0011	TDMIN_BCK	I			
	0100	DMIC_DAT0	I			DMIC DAT0
	0101	UART1_RX	I			UART1 Control
	0110	IR_IN	I			
	0111	CM33_GPIO_EINT10	I			CA33 EINT10
GPIO_B_7	0000	GPIO[19]	I/O	O	PD	GPIO 19
	0001 *	WIFI_TXD	O			
	0010	UART0_RTS	O			UART0 Control
	0011	I2C1_SDA	I			I2C1 Data
	0100	I2SIN_LRCK	O			I2SRX LRCK
	0101	UART1_TX	O			UART1 TX
	0110	PTA_EXT_IF_FREQ	I			
	0111	CM33_GPIO_EINT11	I			CA33 EINT11
GPIO_B_8	0000	GPIO[20]	I/O	I	PD	GPIO 20
	0001 *	CONN_WF_MCU_AICE_TCKC	I			
	0010	UART0_CTS	I			UART0 Control
	0011	I2C1_SCL	I			I2C1 clock
	0100	I2SIN_BCK	O			I2SRX BCK
	0101	DEBUG_12	O			Debug signal
	0110	PTA_EXT_IF_FACT	I			
	0111	CM33_GPIO_EINT12	I			CA33 EINT12
GPIO_B_9	0000	GPIO[21]	I/O	I	PU	GPIO 21
	0001 *	CONN_WF_MCU_AICE_TMSC	I/O			
	0010	PTA_EXT_IF_PRI	I/O			
	0011	TDMIN_LRCK	I/O			
	0100	DMIC_DAT1	I			DMIC DAT1
	0101	DEBUG_13	O			Debug signal
	0110	ANT_SEL9	O			Antenna Select 9
	0111	CM33_GPIO_EINT13	I			CA33 EINT13
GPIO_B_10	0000	GPIO[22]	I/O	I	PD	GPIO 22
	0001 *	CONN_BGF_MCU_AICE_TCKC	I			
	0010	PTA_EXT_IF_WLAN_ACT	O			
	0011	TDMIN_DI	I			
	0100	DMIC_DAT2	I			DMIC Data2
	0101	DEBUG_14	O			Debug signal
	0110	ANT_SEL10	O			Antenna Select 10
	0111	CM33_GPIO_EINT14	I			CA33 EINT14
GPIO_B_11	0000	GPIO[23]	I/O	I	PU	GPIO 23
	0001 *	CONN_BGF_MCU_AICE_TMSC	I/O			
	0010	DSP_URXD0	I			
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	DMIC_DAT3	I			DMIC Data3
	0101	DEBUG_15	O			Debug signal
	0110	ANT_SEL11	O			Antenna Select 11
	0111	CM33_GPIO_EINT15				CA33 EINT15

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IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_12	0000	GPIO[24]	I/O	O	PU	GPIO 24
	0001 *	ADSP_JTAG_TDO	O			DSP JTAG
	0010	DSP_UTXD0	O			
	0011	I2C0_SCL	I/O			I2C0 clock
	0100	DMIC_CLK1	O			DMIC CLK1
	0101	CM33_UART_TX	O			CM33 UART TX
	0110	ANT_SEL12	O			Antenna Select 12
	0111	CM33_GPIO_EINT16	I			CA33 EINT16
GPIO_T_1	0000	GPIO[42]	I/O	I	PD	GPIO 42
	0001	CM33_RSVD1	I			
	0010 *	DBSYS_SWCLK_TCLK	I			CM33 JTAG, CM33_SWD
	0011	UART1_RX	I			UART1 RX
	0100	UART0_RX	I			UART0 RX
	0101	DSP_URXD0	I			
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CA33 EINT1
GPIO_T_3	0000	GPIO[44]	I/O	I	PD	GPIO 44
	0001	CM33_RSDV3	I/O			
	0010 *	DBSYS_SWDIO_TMS	I			CM33 JTAG, CM33_SWD
	0011	UART1_TX	O			UART1 TX
	0100	UART0_TX	O			UART0 TX
	0101	DSP_UTXD0	O			
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT18	I			CA33 EINT18
KPROW_1	0000	GPIO[48]	I/O	I	PU	GPIO 48
	0001 *	CM33_UART_RX	I			
	0010	CM33_TRACE_D2	O			
	0011	KEYPAD_KPROW_1	I/O			
	0100	DSP_URXD0	I			
	0101	PWM_3	O			PWM 3
	0110	ANT_SEL9	O			Antenna Select 9
	0111	AUDIO_DEBUG_IN_0	I			
KPCOL_0	0000	GPIO[50]	I/O	O	PU	GPIO 50
	0001 *	CM33_UART_TX	O			
	0010	CM33_TRACE_D0	O			
	0011	KEYPAD_KPCOL_0	I			
	0100	DSP_UTXD0	O			
	0101	PWM_5	O			PWM 5
	0110	ANT_SEL11	O			Antenna Select 11
	0111	AUDIO_DEBUG_IN_2	I			

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4.8.FTDI debug board

By default, EK-AI7931HD should plug in a FTDI debug board at U69 (Figure 9). Within this FTDI debug board (Figure 9) to make UART signal transfer to USB signal. This debug board also provide a Micro-USB connector to link to with your PC with USB cable

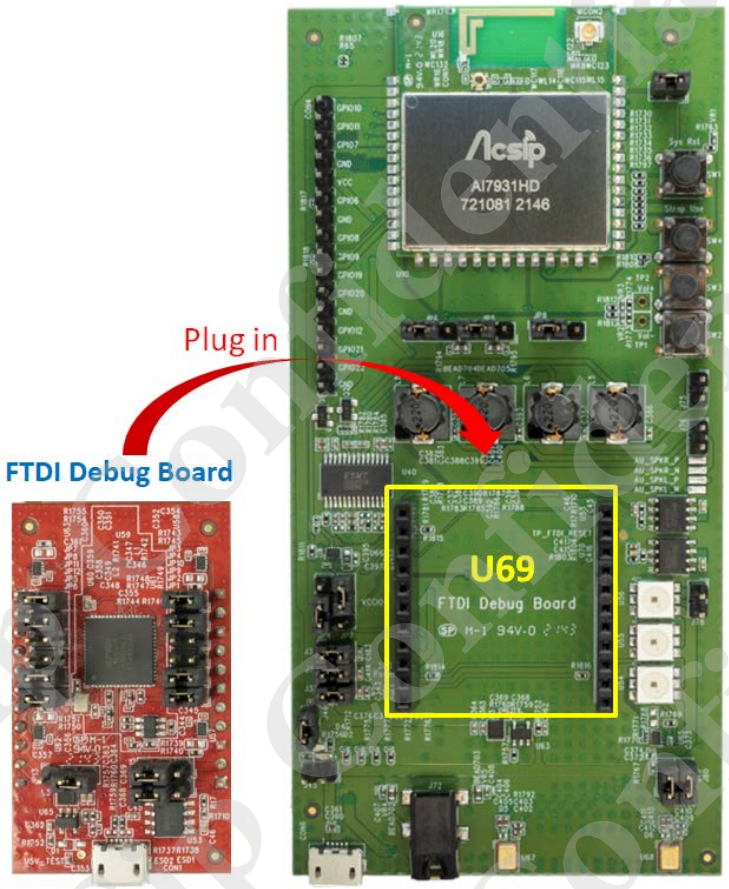

Figure 9. FTDI debug board

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