EK-7933CT
User Guide

Version	A
Doc No	912-13202
Date	2021/12/08

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Document History

Date	Revised Contents	Revised By	Version
2021/12/08	Initial Version	Ivan	A

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1. Introduction

1.1 General Description

MT7933CT is a highly integrated single chip that features an ARM® Cortex-M33 application processor, a low power 1x1 802.11a/b/g/n/ax dual-band Wi-Fi subsystem, a Bluetooth v5.0 subsystem, an Audio subsystem with Cadence® Tensilica® HiFi4 processor and a Power Management Unit (PMU). The Wi-Fi subsystem and a Bluetooth v5.0 subsystem offer feature-rich wireless connectivity at high standards, and deliver reliable, cost- effective throughput from an extended distance. Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. MT7933CT is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

MT7933CT is based on ARM® Cortex-M33 with floating point microcontroller (MCU) including SRAM/ROM memory. The chip also supports rich peripheral interfaces, including USB, UART, SDIO, I2C, SPI, I2S, and auxiliary ADC.

These features are used to download and debug a project on EK-7933CT.

The front view of the HDK including a main board and a FTDI debug board is shown in Figure 1.

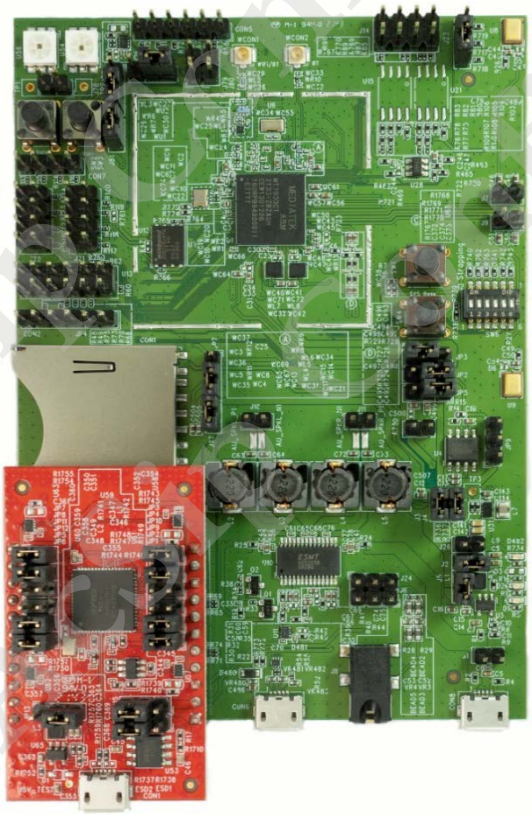

Figure 1. Front view of EK-7933CT and FTDI debug board

2. Get started with the HDK

Before commencing the application development, you need to configure the development platform.

2.1 Configuring the EK-7933CT HDK

EK-7933CT includes a main board and a FTDI Debug board. The top view of the main board is shown in Figure 2.

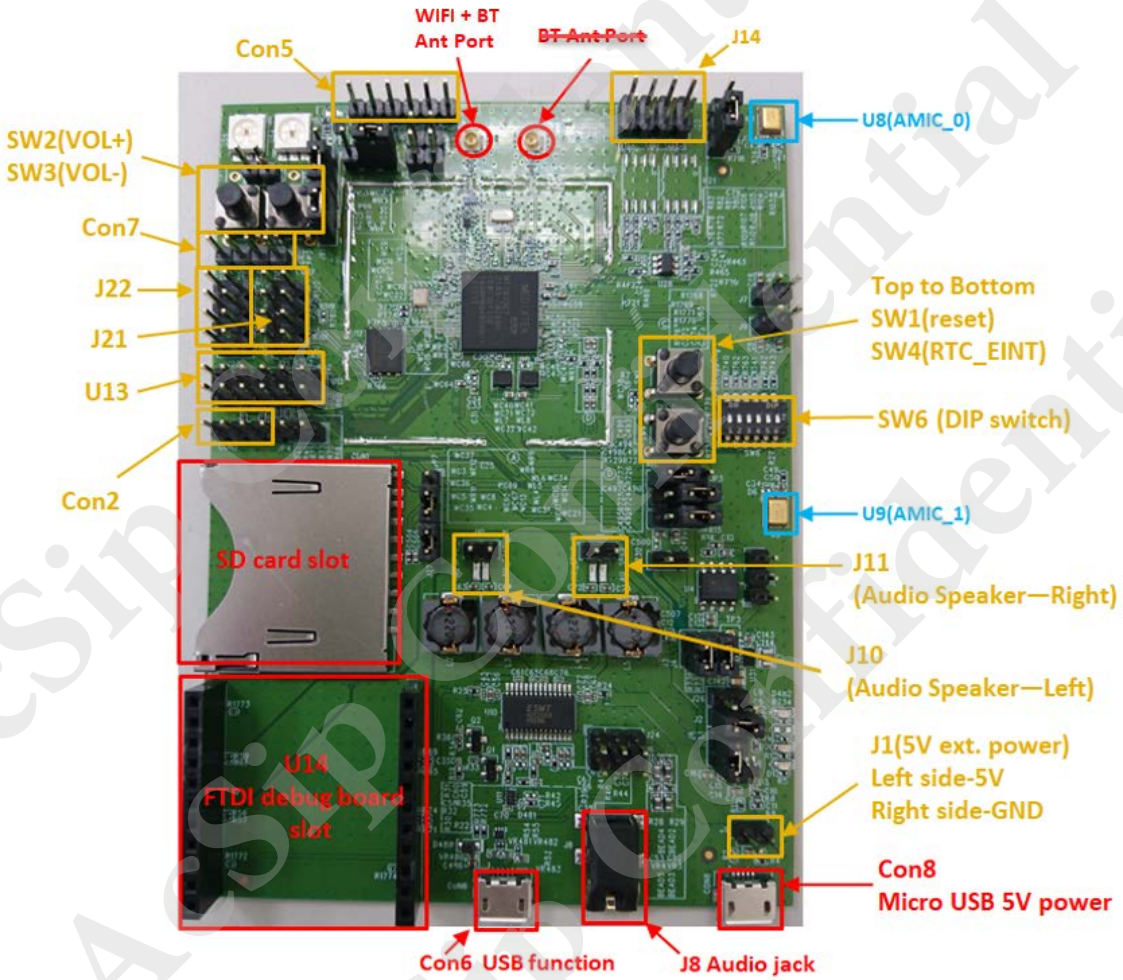

Figure 2. Jumpers and connectors on the EK-7933CT

The description of pins (Figure 2) and their functionality is provided below.

1) CON8 is a USB 5V power for MT7933CT main board, or you can use external 5V power at J1.
2) CON6 is a USB function com port which do not supply 5V power to main board.
3) Press SW1 to reset the system. For SW2~SW6 more detail, please see “section 4.4”.
4) For Wi-Fi and BT function MT7933CT main board reserve a Wi-Fi + BT IPEX connector. Please connect external antenna to transmit and receive RF signals.

5) The FTDI debug board can transfer USB interface to UART interface. Using this debug board can debug through UART, transmit, and receive a signal form PC.

6) U8 and U9 are on-board AMICs which can catch voice command.

7) U10 and U11 are audio speaker connectors which can connect 8ohm/2W speaker to achieve voice assistant function.

The default configuration of the EK-7933CT supports the following functionality:

1) Power supply. Attach a micro-USB connector to the CON8.

2) Supports RTC interrupt.

3) Clock source — 32.768kHz source crystal clock for the RTC mode or external clock operating on 32.768 kHz.

4) XTAL at 26MHz.

2.2 Installing the FTDI debug board drivers on Microsoft Windows

To configure the EK-7933CT HDK:

1) Ensure the FTDI debug board insert to MT7933CT main board at U14.

2) Connect the FTDI debug board to the computer using a micro-USB cable.

3) Connect a 5V power at EK-7933CT CON8 with a micro-USB cable.

4) Check your PC is X86 or X64 system. And download and install FTDI Windows serial port driver from Here. (The red block showed the download file at below figure)

Currently Supported D2XX Drivers:

		Processor Architecture					
Operating System	Release Date	x86 (32-bit)	x64 (64-bit)	ARM	MIPS	SH4	Comments
Windows*	2017-08-30	2.12.28	2.12.28	-	-	-	WHQL Certified. Includes VCP and D2XX. Available as a setup executable Please read the Release Notes and Installation Guides.
Windows RT	2014-07-04	1.0.2	-	1.0.2	-	-	A guide to support the driver (AN_271) is available here
Linux	2018-06-22	1.4.8	1.4.8	1.4.8 ARMv5 soft-float 1.4.8 ARMv5 soft-float uClibc 1.4.8 ARMv6 hard-float *** 1.4.8 ARMv7 hard-float *** 1.4.8 ARMv8 hard-float ***	1.4.8 MIPS32 soft-float 1.4.8 MIPS32 hard-float 1.4.8 MIPS openwrt-uclibc		If unsure which ARM version to use, compare the output of `readelf` and `file` commands on a system binary with the content of release/build/libftd2xx.txt in each package. ReadMe NEW! Video Install Guide

5) If your OS is Windows7 or 10, please open Windows Control Panel then click System and enter Device Manager.

6) In Device Manager, navigate to Ports (COM & LPT) (see Figure 3).

7) A new COM device should appear under Ports (COM & LPT) in Device Manager, as shown in Figure 3. Note the COMx port number of the serial communication port, this information is needed to send command and receive logs from the COM port.

Due to the com port numbers (COMx) are different at different PC. In order to check the function of each com port we can recognize the order of these com ports. As Figure .3 showed, the first com port (#1) means “DSP UART”, the second com port (#2) mean “UART0”, the third com port (#3) mean “UART1”, the fourth com port (#4) mean “CM33 UART”

Figure 3. COM port associated with the EK-7933CT

3. Hardware Features

This section provides the main supported features of the EK-7933CT. The detailed description of the features isprovided in the upcoming sections.

3.1 Features Description

3.1.1 Technology and Package

- 10.6mm x 10.6mm BGA package

3.1.2 Power Management and Clock Source

- Integrates high efficiency power management unit with single 3.3V power supply input
- Supports 26MHz crystal clock with low power operation in idle mode
- Supports 32KHz crystal oscillator or internal 32kHz for low power sleep mode

3.1.3 Platform

- ARM® Cortex-M33 MCU with FPU with up to 300MHz clock speed
- Embedded 1MB SRAM
- Supports external serial flash up to 16MB with eXecute In Place (XIP) and on-the-fly AES
- Supports Hardware crypto engines including AES, DES/3DES, SHA, ECC, TRNG for network security
- Supports up to 47 General Purpose IOs, which are multiplexed with SPI, I2C, Aux ADC, UART, and GPIO interfaces
- Supports 12 DMA channels

3.1.4 Audio

- Cadence® Tensilica® HiFi4 processor with 600MHzclock speed
- Audio Codec with 2 ADC and 1 DAC channels
- Embedded 256KB SRAM memory
- Supports Voice Activity Detection (VAD) and Keyword detection
- On-board headphone jack for external active speaker

3.1.5 Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ax 5GHz and 2.4GHz
- Supports 20MHz, bandwidth in 2.4G/5GHz band, and MCS0~MCS8
- Support MU-MIMO RX
- Support uplink MU-OFDMA TX and downlink MU-OFDMA RX
- Support STBC Rx, LDPC Tx, and RX Beamformed
- Wi-Fi security WFA WPA/WPA2/WPA3 personal
- Support 11ax TWT low power
- Integrated balun, PA, LNA, and T/R switch
- Support antenna diversity

3.1.6 Bluetooth

- Bluetooth v5.0 with 2Mbps PHY rate, Long-range and LE Advertising Extensions
- Integrated balun and PA
- Supports BT/Wi-Fi coexistence

3.1.7 Miscellaneous

- Embedded eFuse to store specific device information and RF calibration data
- Advanced TDD mode Wi-Fi/Bluetooth coexistence scheme

4. Hardware Feature Configuration

4.1 Microcontroller

The MT7933CT features an ARM® Cortex-M33 processor, which is the most energy efficient ARM® processor currently available. It supports the clock rates up to 200MHz when core power is 0.7V and 300MHz when core power is 0.8V. The MCU executes the Thump-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication and bit-field manipulation. The MT7933CT includes a Memory Protection Unit (MPU) in Cortex-M33 MCU to detect unexpected memory access and provides other memory protection features. The MT7933CT also includes FPU in Cortex-M33 MCU.

4.2 Power supply

EK-7933CT supports two types of power supply.

1) Power up with a micro-USB connector.

An on-board switching regulator provides voltage of 3.3V for the EK-7933CT based on MT7933CT, if the power is supplied from an on-board micro-USB connector CON8 (Figure 2). This supply can be isolated from the switching regulator using the jumpers.

Note, that the jumpers J2, J26, J3, J4, JP5 pin1 and pin2, JP2 pin2 and pin3 and JP3 pin2 and pin3 are required to be set on. More details on the jumpers can be found in Table 1.

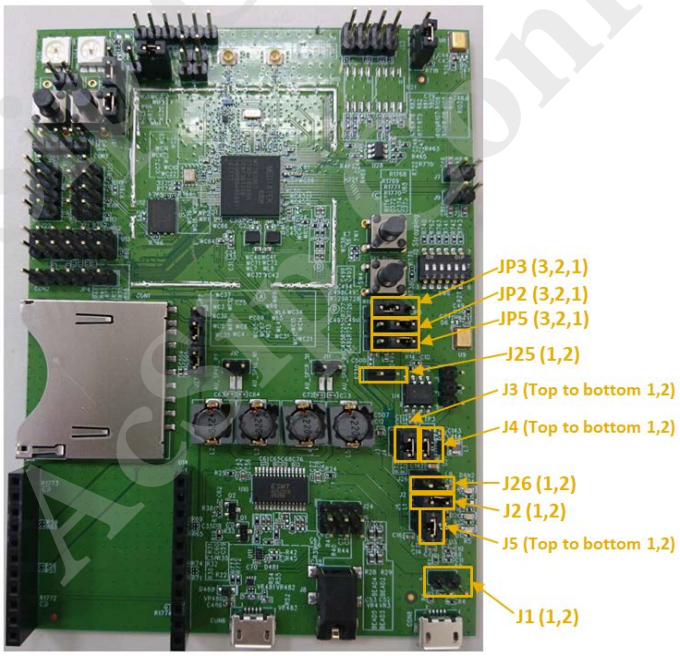

Figure 4. Default power jumper plot

Table 1 Jumper settings for system power input through USB connection

Jumper	Usage	Comments
J1	External 5V power supply	Use external power source to supply 5V voltage to EK-7933CT PCB. Pin 1 is 5V source. Pin2 is GND.
J2	DC-5V transfer to DC-3V3 current source	
J3	Current measurement (3V3)	Measures the current flow in EK-7933CT.
J4	3V3 for external LDO (1.8V and 0.8V)	
J5	3V3 for external components	
J25	AVDD33_VRTC battery power supply	Use AA or AAA battery for RTC 3V3 power. Pin1 is positive endpoint, Pin2 is GND.
J26	Current measurement in RTC mode	Measures the current flow in RTC mode for EK-7933CT.
JP2	Switch VCCIO to 3V3 power domain or 1V8 power domain	Select pin 1 & 2, means VCCIO use 3V3 power domain Select pin 2 & 3, means VCCIO use 1V8 power domain Caution: The flash of EK-7933CT default using3V3 power domain, if you want to change VCCIO to 1V8 power domain please rework flash to 1V8 power domain flash (eq. W25Q128JWPIQ)
JP3	Switch 1V8 VCCIO from internal PHYLDOor external LDO	Select pin 2 & 3, means 1V8 VCCIO from internal PHYLDO Select pin 1 & 2, means 1V8 VCCIO from external Buck component
JP5	Switch RTC 3V3 from DC-3V3 or AVDD33_VRTC	Select pin 1 & 2, means RTC_3V3 use DC-3V3 Select pin 2 & 3, means RTC_3V3 use AVDD33_VRTC

2) Power up using an AA or AAA battery.

- Connect an external AA or AAA battery to battery pin header (J25) to supply power to the system, as shown in Figure 5. When using RTC mode, please note that remove jumper J2 and plug in jumper J26. Jumper JP5 should be switched to pin2 and pin3. More details on the jumpers can be found in.

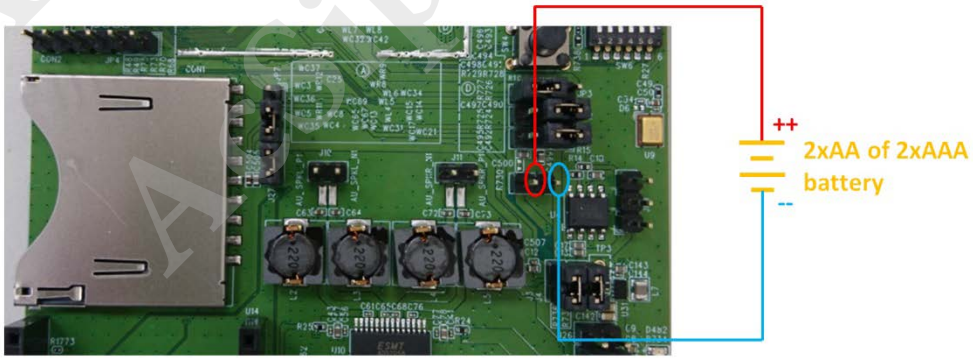

Figure 5. Power up the HDK using an AA or AAA Battery (J25)

4.3 Audio

The EK-7933CT has onboard audio connector associated with different functionalities of the board. The detail of audio related function can refer to Table 2.

Table 2 Audio related function

item	Detail
J8	3.5mm audio jack for external active speaker.
J10	Audio header for left speaker
J11	Audio header for right speaker
U8	AMIC for left channel (the microphone hole is set at back side of EK-7933CT)
U9	AMIC for right channel (the microphone hole is set at back side of EK-7933CT)
SW2	Audio volume up button
SW3	Audio volume down button

4.4 Buttons

The EK-7933CT is equipped with buttons with the following functionality.

The push buttons are shown in Figure 2. The detail of buttons can refer to Table 3.

Table 3 Buttons

Button	Name	Detail
SW1	SYSRST	Press SW1 to restart the EK-7933CT
SW2	Vol+	Audio volume up button
SW3	Vol-	Audio volume down button
SW4	RTC_EINT	Press SW4 to enable RTC mode
SW6	DIP switch	Slide the DIP switch to trigger strapping mode (download mode…)

4.5 SD card

The EK-7933CT reserve a SD card slot to provide user to save data into a SD card. And note that there are some registers which placed at bask side need to be reworked before using SD card. Please refer to figure.6.

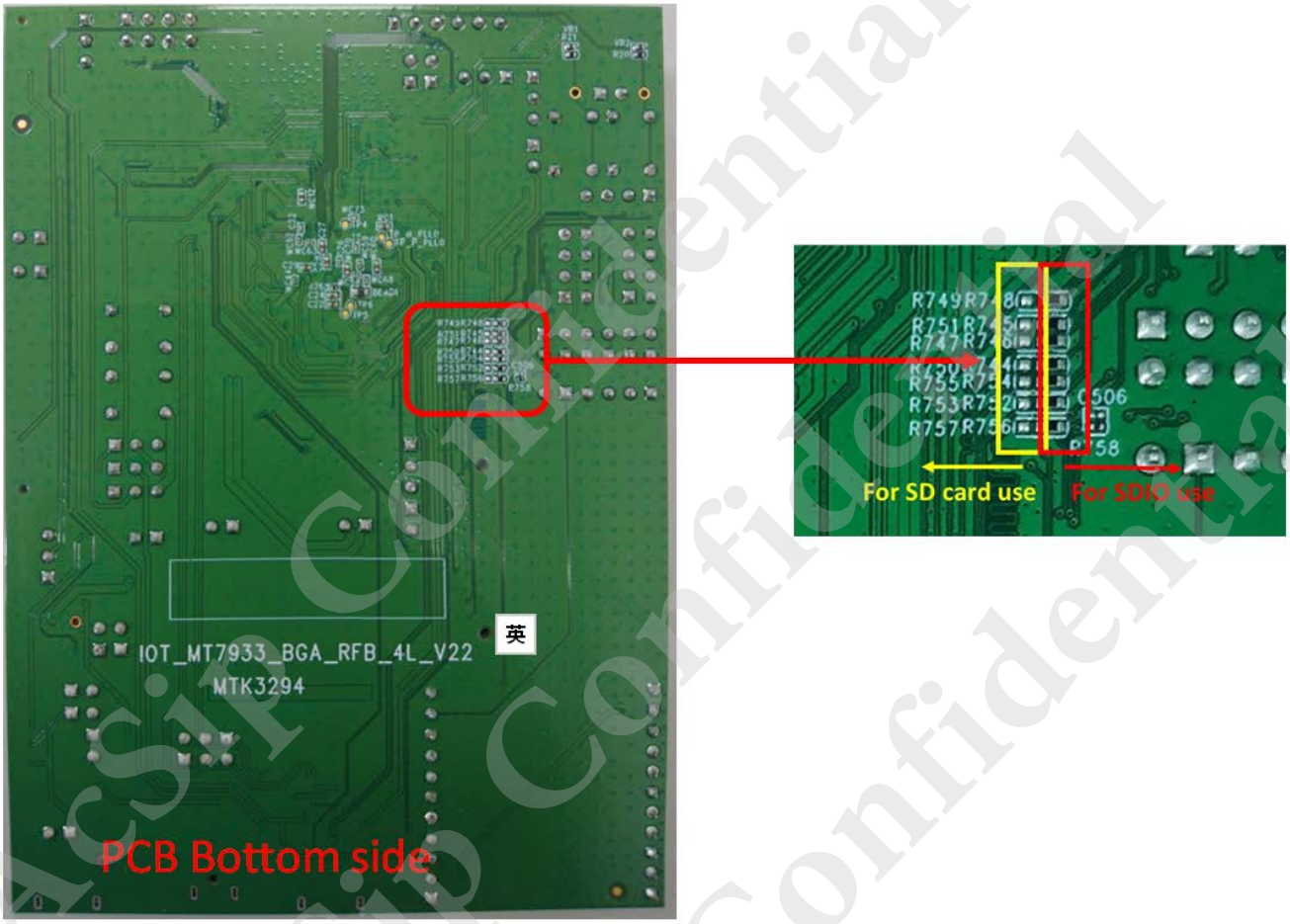

Figure 6. SD card slot rework

For SD Card Use	For SDIO Use
R749=0R, R748=NC	R749=NC, R748=0R
R751=0R, R745=NC	R751=NC, R745=0R
R747=0R, R746=NC	R747=NC, R746=0R
R750=0R, R744=NC	R750=NC, R744=0R
R755=0R, R754=NC	R755=NC, R754=0R
R753=0R, R752=NC	R753=NC, R752=0R
R757=0R, R756=NC	R757=NC, R756=0R

4.6 Extension connectors

The EK-7933CT provides similar pin-out extension connectors for various sensor and device connectivity, as shown in Figure.7 and described in Table 4.

The board has 30 GPIOs multiplexed with other interfaces. Depending on the use case, user can configure each I/Ofunctionality.

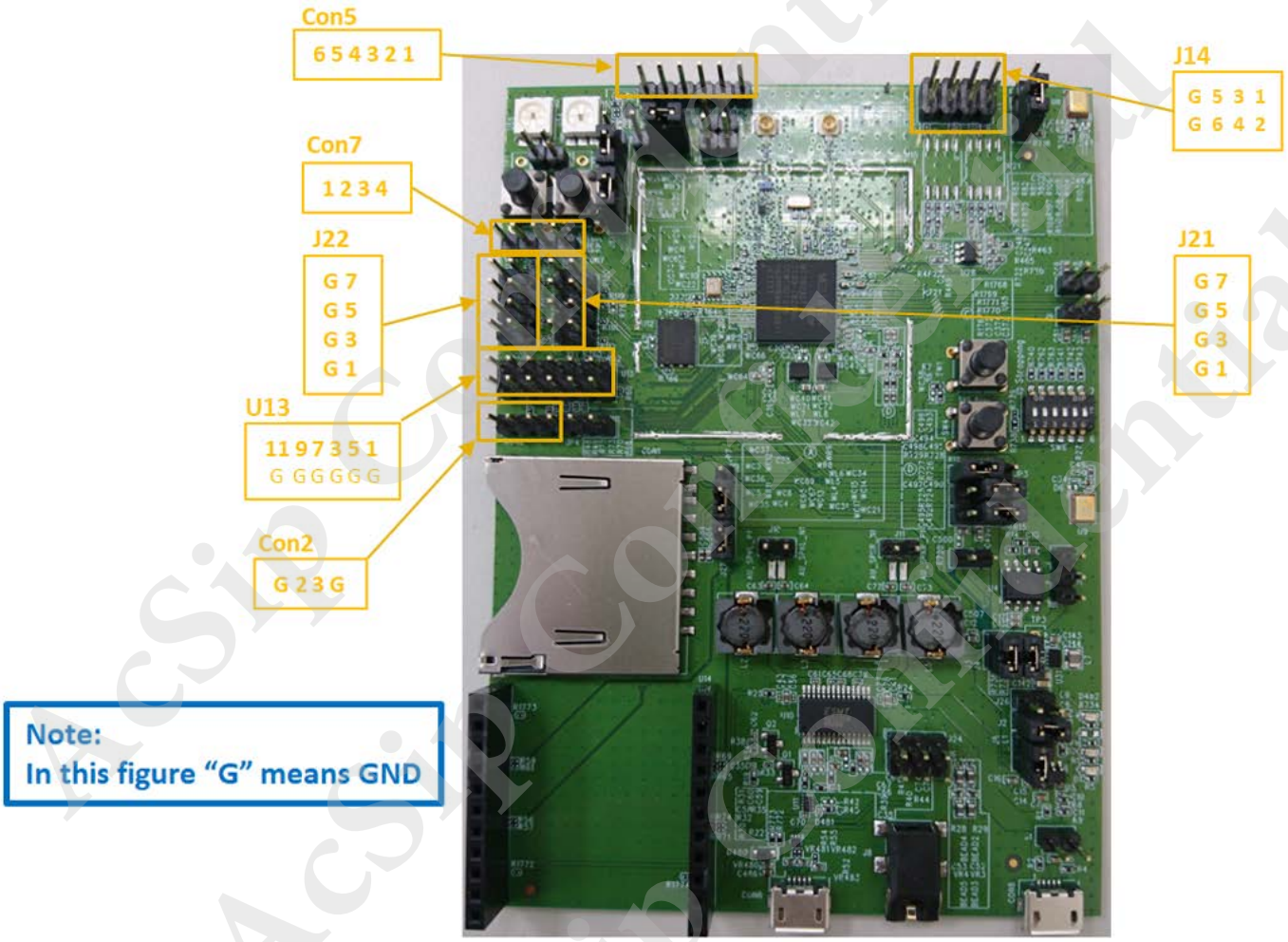

Figure 7. GPIO pin-out extension connectors

Table 4 GPIO pin-out extension connectors

Signal Name	Connector Pin Number	Signal Name	Connector Pin Number
GPIO_0	Reserve for flash	GPIO_27	CON2 - 2
GPIO_1	Reserve for flash	GPIO_28	CON2 - 3
GPIO_2	Reserve for flash	GPIO_29	Reserve for DSP UART
GPIO_3	Reserve for flash	GPIO_30	Reserve for DSP UART
GPIO_4	Reserve for flash	GPIO_31	Reserve for USB
GPIO_5	Reserve for flash	GPIO_32	Reserve for USB
GPIO_6	CON7 – 1 (R747=NC, R746=0R)	GPIO_33	Reserve for USB
GPIO_7	CON7 – 2 (R749=NC, R748=0R)	GPIO_34	Reserve for USB
GPIO_8	CON7 – 3 (R750=NC, R744=0R)	GPIO_35	J14 - 2
GPIO_9	CON7 – 4 (R751=NC, R745=0R)	GPIO_36	J14 - 1
GPIO_10	J21 – 1 (R753=NC, R752=0R)	GPIO_37	J14 - 4
GPIO_11	J22 – 1 (R755=NC, R754=0R)	GPIO_38	J14 - 3
GPIO_12	MSDC0_RST (R757=0R, R756=NC)	GPIO_39	J14 - 6
GPIO_13	J22 - 3	GPIO_40	J14 - 5
GPIO_14	J22 - 5	GPIO_41	Reserve for I2C
GPIO_15	J22 - 7	GPIO_42	Reserve for UART1
GPIO_16	J21 - 7	GPIO_43	Reserve for I2C
GPIO_17	U13 - 1	GPIO_44	Reserve for UART1
GPIO_18	U13 - 3	GPIO_45	Reserve for I2C
GPIO_19	J21 - 5	GPIO_46	Reserve for I2C
GPIO_20	J21 - 3	GPIO_47	CON5 - 1
GPIO_21	U13 - 5	GPIO_48	Reserve for CM33 UART
GPIO_22	U13 - 7	GPIO_49	CON5 - 3
GPIO_23	U13 - 9	GPIO_50	Reserve for CM33 UART
GPIO_24	U13 - 11	GPIO_51	CON5 - 5
GPIO_25	Reserve for UART0	GPIO_52	CON5 - 6
GPIO_26	Reserve for UART0		

Table 5 GPIO pin multi-function definition

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
PAD_SYSRST_B	NA	PAD_SYSRST_B			PU	Chip hardware
SDIO_CLK	0000	GPIO[6]	I/O	I	PD	GPIO 6
	0001 *	SDIO_CLK	I			SDIO Clock
	0010	MSDC0_CLK	O			MSDC Clock
	0011	SPIM0_SCK	O			SPI0 (Master) Clock
	0100	CM33_GPIO_EINT0	I			CA33 EINT0
	0101	DEBUG_0	O			Debug signal
	0110	ANT_SEL0	O			Antenna Select 0
	0111	BGF_EINT_10_B	I			
SDIO_CMD	0000	GPIO[7]	I/O	I	PU	GPIO 7
	0001 *	SDIO_CMD	I/O			SDIO Command
	0010	MSDC0_CMD	I/O			
	0011	SPIM0_CS_N	O			SPI0 (Master) Chip Select
	0100	CM33_GPIO_EINT1	I			CA33 EINT1
	0101	DEBUG_1	O			Debug signal
	0110	ANT_SEL1	O			Antenna Select 1
	0111	PINMUX_EXT_INT_N_IN	I			
SDIO_DAT0	0000	GPIO[8]	I/O	I	PU	GPIO 8
	0001 *	SDIO_DAT0	O			SDIO Data[0]
	0010	MSDC0_DAT0	I/O			MSDC0 data0
	0011	SPIM0_MISO	I			SPI0 (Master) Input
	0100	UART0_RTS	O			
	0101	DEBUG_2	O			Debug signal
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CA33 EINT0
SDIO_DAT1	0000	GPIO[9]	I/O	I	PU	GPIO 9
	0001 *	SDIO_DAT1	I/O			SDIO Data[1]
	0010	MSDC0_DAT1	I/O			MSDC0 data1
	0011	SPIM0_MOSI	O			SPI0 (Master) Output
	0100	UART0_CTS	I			UART0 Control
	0101	DEBUG_3	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CA33 EINT1
SDIO_DAT2	0000	GPIO[10]	I/O	I	PU	GPIO 10
	0001 *	SDIO_DAT2	I/O			SDIO Data[2]
	0010	MSDC0_DAT2	I/O			MSDC0 data2
	0011	I2SIN_DAT0	I			
	0100	UART0_RX	I			UART0 RX
	0101	DEBUG_4	O			Debug signal
	0110	I2C0_SCL	I/O			
	0111	CM33_GPIO_EINT2	I			CA33 EINT2
SDIO_DAT3	0000	GPIO[11]	I/O	I	PU	GPIO 11
	0001 *	SDIO_DAT3	I/O			SDIO Data[3]
	0010	MSDC0_DAT3	I/O			
	0011	I2SO_DAT0	O			I2SO Data
	0100	UART0_TX	O			UART0 TX
	0101	DEBUG_5	O			Debug signal
	0110	I2C0_SDA	I			I2C0 Data
	0111	CM33_GPIO_EINT3	I			CA33 EINT3

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_0	0000	GPIO[12]	I/O	O	PU	GPIO 12
	0001 *	CONN_BGF_UART0_TXD	O			
	0010	MSDC0_RST	O			MSDC0 reset
	0011	CONN_BT_TXD	O			
	0100	WIFI_TXD	O			
	0101	DEBUG_6	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT4	I			CA33 EINT4
GPIO_B_1	0000	GPIO[13]	I/O	I	PU	GPIO 13
	0001 *	USB_IDDIG	I			USB OTG ID pin
	0010	SPIM1_SCK	O			SPIM1 (Master) Clock
	0011	I2SO_BCK	O			I2SO BCK
	0100	UART1_RX	I			UART1 RX
	0101	DEBUG_7	O			
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT5	I			CA33 EINT5
GPIO_B_2	0000	GPIO[14]	I/O	O	PD	GPIO 14
	0001 *	USB_DRV_VBUS	O			USB OTG host mode
	0010	SPIM1_MOSI	O			SPI1 (Master) Output
	0011	I2SO_LRCK	O			I2SO LRCK
	0100					
	0101	DEBUG_8	O			Debug signal
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT6	I			CA33 EINT6
GPIO_B_3	0000	GPIO[15]	I/O	I	PD	GPIO 15
	0001 *	USB_OC	I			USB Host mode over-
	0010	SPIM1_MISO	I			SPI1 (Master) Input
	0011	I2SO_MCK	O			I2STX MCLK
	0100	I2SIN_MCK	O			I2SRX MCK
	0101	DEBUG_9	O			Debug signal
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT7	I			CA33 EINT7
GPIO_B_4	0000	GPIO[16]	I/O	I	PD	GPIO 16
	0001 *	USB_VBUS_VALID	I			USB device mode VBUS detect
	0010	SPIM1_CS_N	O			SPI1 (Master) Chip Select
	0011	IR_IN	I			
	0100	I2SIN_MCK	O			I2SRX MCLK
	0101	DEBUG_10	O			Debug signal
	0110	ANT_SEL7	O			Antenna Select 7
	0111	CM33_GPIO_EINT8	I			CA33 EINT8
GPIO_B_5	0000	GPIO[17]	I/O	I	PU	GPIO 17
	0001 *	CONN_BGF_UART0_RXD	I			
	0010	UART0_RX	I			UART0 RX
	0011	TDMIN_MCLK	I			
	0100	DMIC_CLK0	O			DMIC CLK0
	0101	DEBUG_11	O			Debug signal
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT9	I			CA33 EINT9

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_6	0000	GPIO[18]	I/O	O	PU	GPIO 18
	0001 *	CONN_BT_TXD	O			
	0010	UART0_TX	O			UART0 TX
	0011	TDMIN_BCK	I			
	0100	DMIC_DAT0	I			DMIC DAT0
	0101	UART1_RX	I			UART1 Control
	0110	IR_IN	I			
	0111	CM33_GPIO_EINT10	I			CA33 EINT10
GPIO_B_7	0000	GPIO[19]	I/O	O	PD	GPIO 19
	0001 *	WIFI_TXD	O			
	0010	UART0_RTS	O			UART0 Control
	0011	I2C1_SDA	I			I2C1 Data
	0100	I2SIN_LRCK	O			I2SRX LRCK
	0101	UART1_TX	O			UART1 TX
	0110	PTA_EXT_IF_FREQ	I			
	0111	CM33_GPIO_EINT11	I			CA33 EINT11
GPIO_B_8	0000	GPIO[20]	I/O	I	PD	GPIO 20
	0001 *	CONN_WF_MCU_AICE_TCK	I			
	0010	UART0_CTS	I			UART0 Control
	0011	I2C1_SCL	I			I2C1 clock
	0100	I2SIN_BCK	O			I2SRX BCK
	0101	DEBUG_12	O			Debug signal
	0110	PTA_EXT_IF_FACT	I			
	0111	CM33_GPIO_EINT12	I			CA33 EINT12
GPIO_B_9	0000	GPIO[21]	I/O	I	PU	GPIO 21
	0001 *	CONN_WF_MCU_AICE_TMS	I/O			
	0010	PTA_EXT_IF_PRI	I/O			
	0011	TDMIN_LRCK	I/O			
	0100	DMIC_DAT1	I			DMIC DAT1
	0101	DEBUG_13	O			Debug signal
	0110	ANT_SEL9	O			Antenna Select 9
	0111	CM33_GPIO_EINT13	I			CA33 EINT13
GPIO_B_10	0000	GPIO[22]	I/O	I	PD	GPIO 22
	0001 *	CONN_BGF_MCU_AICE_TCK	I			
	0010	PTA_EXT_IF_WLAN_ACT	O			
	0011	TDMIN_DI	I			
	0100	DMIC_DAT2	I			DMIC Data2
	0101	DEBUG_14	O			Debug signal
	0110	ANT_SEL10	O			Antenna Select 10
	0111	CM33_GPIO_EINT14	I			CA33 EINT14
GPIO_B_11	0000	GPIO[23]	I/O	I	PU	GPIO 23
	0001 *	CONN_BGF_MCU_AICE_TM	I/O			
	0010	DSP_URXD0	I			
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	DMIC_DAT3	I			DMIC Data3
	0101	DEBUG_15	O			Debug signal
	0110	ANT_SEL11	O			Antenna Select 11
	0111	CM33_GPIO_EINT15				CA33 EINT15

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_12	0000	GPIO[24]	I/O	O	PU	GPIO 24
	0001 *	ADSP_JTAG_TDO	O			DSP JTAG
	0010	DSP_UTXD0	O			
	0011	I2C0_SCL	I/O			I2C0 clock
	0100	DMIC_CLK1	O			DMIC CLK1
	0101	CM33_UART_TX	O			CM33 UART TX
	0110	ANT_SEL12	O			Antenna Select 12
	0111	CM33_GPIO_EINT16	I			CA33 EINT16
GPIO_B_13	0000	GPIO[25]	I/O	I	PD	GPIO 25
	0001 *	ADSP_JTAG_TCK	I			DSP JTAG
	0010	CM33_UART_RX	I			CM33 UART RX
	0011	UART0_RX	I			UART0 Control
	0100	SPIM0_SCK	O			SPIM0 clock
	0101					
	0110	UART1_RX	I			UART1 RX
	0111	CM33_GPIO_EINT17	I			CA33 EINT17
GPIO_B_14	0000	GPIO[26]		I	PU	GPIO 26
	0001 *	ADSP_JTAG_TRST	I			DSP JTAG
	0010	CM33_UART_TX	O			CM33 UART TX
	0011	UART0_TX	O			UART0 TX
	0100	SPIM0_CS_N	O			SPIM0 CS
	0101					
	0110	UART1_TX	O			UART1 TX
	0111	CM33_GPIO_EINT18	I			CA33 EINT18
GPIO_B_15	0000	GPIO[27]	I/O	I	PU	GPIO 27
	0001 *	ADSP_JTAG_TDI	I			DSP JTAG
	0010	CM33_UART_RTS	O			CM33 UART RTS
	0011	UART0_RTS	O			UART0 RTS
	0100	SPIM0_MISO	I			SPIM0 MISO
	0101					
	0110	UART1_RTS	O			UART1 Control
	0111	CM33_GPIO_EINT19	I			CA33 EINT19
GPIO_B_16	0000	GPIO[28]	I/O	I	PU	GPIO 28
	0001 *	ADSP_JTAG_TMS	I			DSP JTAG
	0010	CM33_UART_CTS	I			CM33 UART CTS
	0011	UART0_CTS	I			UART0 Control
	0100	SPIM0_MOSI	O			SPIM0 MOSI
	0101	SPIS_MISO	O			SPIS MISO
	0110	UART1_CTS	I			UART1 Control
	0111	CM33_GPIO_EINT20	I			CA33 EINT20

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_R_0	0000	GPIO[29]	I/O	I	PU	GPIO29
	0001 *	DSP_URXD0	I			
	0010	ADSP_JTAG_TDO	O			DSP JTAG
	0011	PWM_0	O			PWM0
	0100	PTA_EXT_IF_PRI	I/O			
	0101	CONN_WF_MCU_TDO	O			
	0110	CM33_RSVD1	I			
	0111	CM33_GPIO_EINT21	I			CA33 EINT21
GPIO_R_1	0000	GPIO[30]	I/O	O	PD	GPIO 30
	0001 *	DSP_UTXD0	O			
	0010	ADSP_JTAG_TCK	I			DSP JTAG
	0011	PWM_1	O			PWM 1
	0100	PTA_EXT_IF_WLAN_ACT	O			
	0101	CONN_WF_MCU_TCK	I			
	0110	CM33_RSVD3	I/O			
	0111	CM33_GPIO_EINT22	I			CA33 EINT22
GPIO_R_2	0000	GPIO[31]	I/O	O	PD	GPIO 31
	0001 *	USB_DRV_VBUS	O			USB Host mode VBUS driving
	0010	ADSP_JTAG_TRST	I			DSP JTAG
	0011	PWM_2	O			PWM2
	0100	PTA_EXT_IF_FREQ	I			
	0101	CONN_WF_MCU_TDI	I			
	0110	CM33_RSVD0	I			
	0111	CM33_GPIO_EINT23	I			CA33 EINT23
GPIO_R_3	0000	GPIO[32]	I/O	I	PD	GPIO 32
	0001 *	USB_OC	I			USB Host mode over-current
	0010	ADSP_JTAG_TDI	I			DSP JTAG
	0011	PWM_3	O			PWM3
	0100	PTA_EXT_IF_ACT	I			
	0101	CONN_WF_MCU_TRSR_B	I			
	0110	CM33_RSVD2	I			
	0111	CM33_GPIO_EINT24	I			CA33 EINT24
GPIO_R_4	0000	GPIO[33]	I/O	I	PD	GPIO 33
	0001 *	USB_VBUS_VALID	I			USB device mode VBUS detect
	0010	ADSP_JTAG_TMS	I			DSP JTAG
	0011	PWM_4	O			PWM 4
	0100	I2C1_SDA	I			I2C1 Data
	0101	CONN_WF_MCU_TMS	I			
	0110	CM33_RSVD4	O			
	0111	CM33_GPIO_EINT25	I			CA33 EINT25
GPIO_R_5	0000	GPIO[34]	I/O	I	PU	GPIO 34
	0001 *	USB_IDDIG	I			USB OTG ID pin
	0010	I2C0_SCL	I			I2C0 clock
	0011	PWM_5	O			PWM 5
	0100	I2C1_SCL	I			I2C1 clock
	0101	EXT_CK	I			
	0110	DEBUG_0	O			Debug signal
	0111	CM33_GPIO_EINT26	I			CA33 EINT26

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_R_6	0000	GPIO[35]	I/O	O	PD	GPIO 35
	0001 *	UART0_TX	O			UART0 TX
	0010	CM33_UART_RTS	O			CM33 UART RTS
	0011	PWM_6	O			PWM 6
	0100	PWM_2	O			PWM 2
	0101	CONN_BGF_MCU_TDO	O			
	0110	DEBUG_1	O			Debug signal
	0111	CM33_GPIO_EINT27	I			CA33 EINT27
GPIO_R_7	0000 *	GPIO[36]	I/O	I	PD	GPIO 36
	0001	DBSYS_NTRST	I			
	0010	CM33_UART_CTS	I			CM33 UART CTS
	0011	PWM_7	O			PWM 7
	0100	PWM_3	O			PWM 3
	0101	CONN_BGF_MCU_TCK	I			
	0110	DEBUG_2	O			Debug signal
	0111	CM33_GPIO_EINT28	I			CA33 EINT28
GPIO_R_8	0000 *	GPIO[37]	I/O	I	PD	GPIO 37
	0001	DBSYS_SWCLK_TCLK	I			
	0010	I2C1_SDA	I			I2C1
	0011	PWM_8	O			PWM 8
	0100	I2C0_SDA				I2C 0
	0101	CONN_BGF_MCU_TDI	I			
	0110	DEBUG_3	O			Debug signal
	0111	CM33_GPIO_EINT29	I			CA33 EINT29
GPIO_R_9	0000 *	GPIO[38]	I/O	I	PD	GPIO 38
	0001	DBSYS_TDI	I			
	0010	CM33_UART_TX	O			CM33 UART TX
	0011	PWM_9	O			PWM 9
	0100	I2C0_SDA	I/O			I2C0 Data
	0101	CONN_BGF_MCU_TRS	I			
	0110	I2C1_SCL	I/O			I2C1
	0111	CM33_GPIO_EINT30	I			CA33 EINT30
GPIO_R_10	0000 *	GPIO[39]	I/O	I	PD	GPIO 39
	0001	DBSYS_SWDIO_TMS	I/O			
	0010	I2C0_SDA	I			I2C0 Data
	0011	PWM_10	O			PWM 10
	0100	DSP_URXD0	I			
	0101	CONN_BGF_MCU_TMS	I			
	0110	ANT_SEL0	O			Antenna Select 0
	0111	BGF_EINT_10_B	I			
GPIO_R_11	0000 *	GPIO[40]	I/O	O	PU	GPIO 40
	0001	DBSYS_TDO	O			
	0010	CM33_UART_RX	I			
	0011	PWM_11	O			PWM 11
	0100	DSP_UTXD0	O			
	0101	UART0_RX	I			UART0 RX
	0110	ANT_SEL1	O			Antenna Select 1
	0111	PINMUX_EXT_INT_N_I	I			

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_T_0	0000	GPIO[41]	I/O	I	PD	GPIO 41
	0001	CM33_RSVD0	I			
	0010 *	DBSYS_NTRST	I			CM33 JTAG
	0011	I2C0_SDA	I			I2C0 Data
	0100	CONN_BGF_UART0_RX	I			
	0101	I2C1_SDA	1			I2C1 Data
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CA33 EINT0
GPIO_T_1	0000	GPIO[42]	I/O	I	PD	GPIO 42
	0001	CM33_RSVD1	I			
	0010 *	DBSYS_SWCLK_TCLK	I			CM33 JTAG, CM33_SWD
	0011	UART1_RX	I			UART1 RX
	0100	UART0_RX	I			UART0 RX
	0101	DSP_URXD0	I			
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CA33 EINT1
GPIO_T_2	0000	GPIO[43]	I/O	I	PD	GPIO 43
	0001	CM33_RSVD2	I			
	0010 *	DBSYS_TDI	I			CM33 JTAG
	0011	I2C0_SCL	I			I2C0 clock
	0100	CONN_BGF_UART0_TX	O			
	0101	I2C1_SCL	1			I2C1 clock
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT17	I			CA33 EINT17
GPIO_T_3	0000	GPIO[44]	I/O	I	PD	GPIO 44
	0001	CM33_RSDV3	I/O			
	0010 *	DBSYS_SWDIO_TMS	I			CM33 JTAG, CM33_SWD
	0011	UART1_TX	O			UART1 TX
	0100	UART0_TX	O			UART0 TX
	0101	DSP_UTXD0	O			
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT18	I			CA33 EINT18
GPIO_T_4	0000	GPIO[45]	I/O	O	PU	GPIO 45
	0001	CM33_RSVD4	O			
	0010 *	DBSYS_TDOO	O			CM33 JTAG
	0011	I2C1_SDA	I			I2C1 Data
	0100	WIFI_TXD	O			
	0101	PWM_0	O			PWM0
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT19	I			CA33 EINT19
GPIO_T_5	0000	GPIO[46]	I/O	O	PU	GPIO 46
	0001 *	SPIM0_SCK	O			SPIM0 SCK
	0010	CM33_TRACE_CLK	O			
	0011	I2C1_SCL	I			I2C1
	0100	ONN_WF_MCU_AICE_	I			
	0101	PWM_1	O			PWM 1
	0110	ANT_SEL7	O			Antenna Select 7
	0111					

IO Name	CR Value default*	Name	Dir	Default		Description
				Dir	PU/PD	
KPROW_0	0000	GPIO[47]	I/O	O	PU	GPIO 47
	0001 *	SPIM0_CS_N	O			SPIM0 CS
	0010	CM33_TRACE_D3	O			
	0011	KEYPAD_KPROW_0	I/O			
	0100	CONN_WF_MCU_AICE_TMSC	I/O			
	0101	PWM_2	O			PWM 2
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT2	I			CA33 EINT2
KPROW_1	0000	GPIO[48]	I/O	I	PU	GPIO 48
	0001 *	CM33_UART_RX	I			
	0010	CM33_TRACE_D2	O			
	0011	KEYPAD_KPROW_1	I/O			
	0100	DSP_URXD0	I			
	0101	PWM_3	O			PWM 3
	0110	ANT_SEL9	O			Antenna Select 9
	0111	AUDIO_DEBUG_IN_0	I			
KPROW_2	0000	GPIO[49]	I/O	O	PU	GPIO 49
	0001 *	CM33_UART_TX	O			
	0010	CM33_TRACE_D1	O			
	0011	KEYPAD_KPROW_2	I/O			
	0100	CONN_BT_TXD	O			
	0101	PWM_4	O			PWM 4
	0110	ANT_SEL10	O			Antenna Select 10
	0111	AUDIO_DEBUG_IN_1	I			
KPCOL_0	0000	GPIO[50]	I/O	O	PU	GPIO 50
	0001 *	CM33_UART_TX	O			
	0010	CM33_TRACE_D0	O			
	0011	KEYPAD_KPCOL_0	I			
	0100	DSP_UTXD0	O			
	0101	PWM_5	O			PWM 5
	0110	ANT_SEL11	O			Antenna Select 11
	0111	AUDIO_DEBUG_IN_2	I			
KPCOL_1	0000	GPIO[51]	I/O	I	PD	GPIO 51
	0001 *	SPIM0_MISO	I			SPIM0 MISO
	0010	CM33_SWO	O			
	0011	KEYPAD_KPCOL_1	I			
	0100	CONN_BGF_MCU_AICE_TCKC	I			
	0101	PWM_6	O			PWM 6
	0110	ANT_SEL12	O			Antenna Select 12
	0111	AUDIO_DEBUG_IN_3	I			
KPCOL_2	0000	GPIO[52]	I/O	O	PU	GPIO 52
	0001 *	SPIM0_MOSI	O			SPIM0 MOSI
	0010	CM33_UART_RX	I			CM33 UART RX
	0011	KEYPAD_KPCOL_2	I			
	0100	CONN_BGF_MCU_AICE_TCKC	I/O			
	0101	PWM_7	O			PWM 7
	0110	UART1_TX	O			UART1 TX
	0111	AUDIO_DEBUG_IN_4	I			

4.7 RTC

The EK-7933CT features a RTC module The clock source operates at 32.768kHz crystal oscillator or an external clock source The RTC has built-in accurate timer to wake up the system when the user-defined timer expires The RTC uses a different power source from the Power Management Unit (PMU) In retention mode, the PMU is turned off while the RTC module remains powered on The RTC module only consumes 3μA in retention mode The RTC has a dedicated PMU control pin RTC_PMU_EN (pin F12) used to turn the power on when the RTC timer expires and turn the power off when it intends to enter the hibernate mode

4.8 FTDI debug board

By default, EK-7933CT should plug in a FTDI debug board at U14 (Figure 8). Within this FTDI debug board to make UART signal transfer to USB signal This debug board also provide a Micro-USB connector to link to with your PC with USB cable.

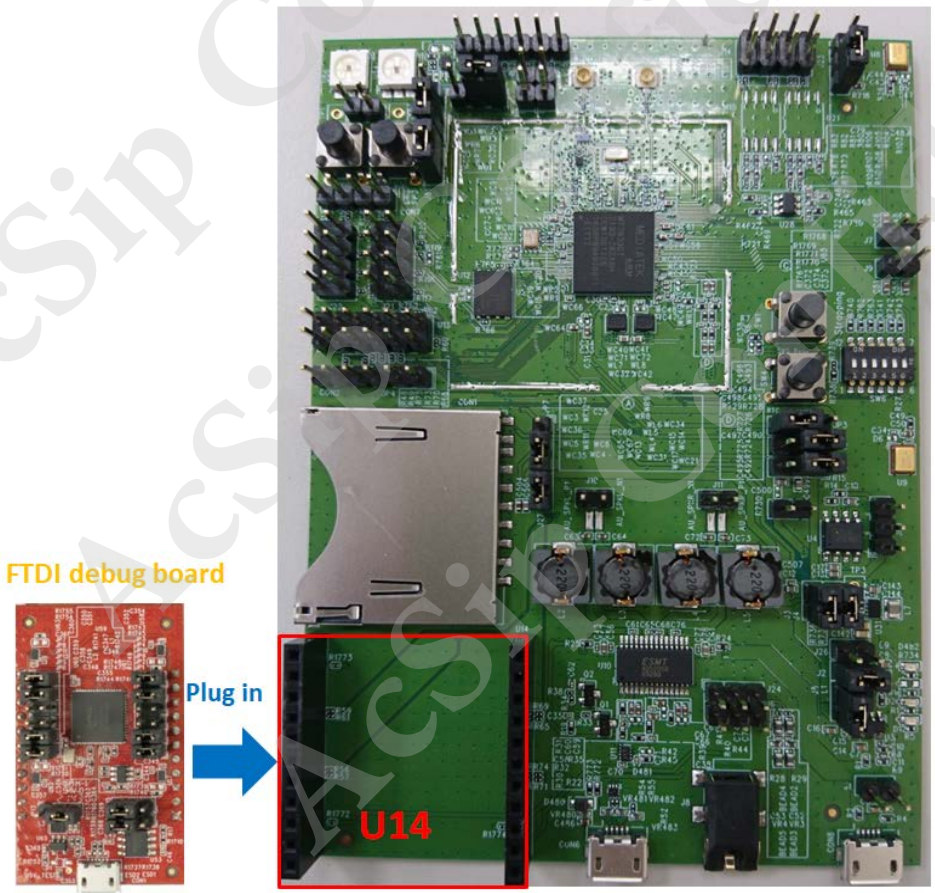

Figure 8. FTDI debug board