PRODUCT SPECIFICATION

Product Name	ST50H LoRa Wireless Communication Module
Version	D
Doc No	901-12601
Date	2021/05/21

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Document History

Date	Revised Contents	Revised By	Version
2020/03/26	Initial release	PW	A
2020/05/08	Update Pin Definition	PW	B
2020/11/03	Modify TX/RX Spec.	Jack	C
2021/05/21	Modify Tx Power Spec.	Jack	D

1. General Description

The ST50H integrates ARM Coretex®-M4 (32-bit RISC core operating at a frequency of up to 48 MHz) MCU with LoRa modulation that provides ultra-long range spread spectrum communication and high interference immunity whilst minimizing current consumption.

The ST50H can achieve a sensitivity of over -136 dBm. The high sensitivity combined with the integrated +21 dBm power amplifier yields industry leading link budget making it optimal for any low data rate application requiring range or robustness. LoRa also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference immunity and energy consumption.

➢ Feature:

- Chipset: STM32WLE5(single core)
- High performance ARM® Cortex®-M4 32-bit RISC core operating up to 48 MHz frequency
- Embedded memories (256 Kbytes of Flash memory and 64 Kbytes of RAM)
- Hardware encryption AES 256-bit
- True random number generator (RNG)
- CRC calculation unit
- Unique device identifier (64-bit UID compliant with IEEE 802-2001 standard)
- 96-bit unique die identifier
- Hardware public key accelerator (PKA)
- 32 MHz TCXO & 32 KHz XTAL
- 2 DMA, 2 USART, 1 LPUART, 2 SPI, 3 I2C
- RTC wakeup counter, SysTick, Watchdog
- Modulation: LoRa®, (G)FSK, (G)MSK and BPSK
- +22 dBm Max. RF output
- Programmable bit rate up to 300 kbps
- High sensitivity: down to -138 dBm for LoRa @125kHz, SF12
- Automatic RF Sense and CAD with ultra-fast AFC
- Small footprint：12 mm x 12 mm x 1.22 mm(Typ.)
- High-efficiency SMPS step-down converter and independent power supplies for ADC, DAC and comparator analog inputs.
- VBAT mode with RTC and 20x32-byte backup registers, battery voltage monitoring

1-1. Block Diagram

A simplified block diagram of the ST50H module is depicted as figure 1 below.

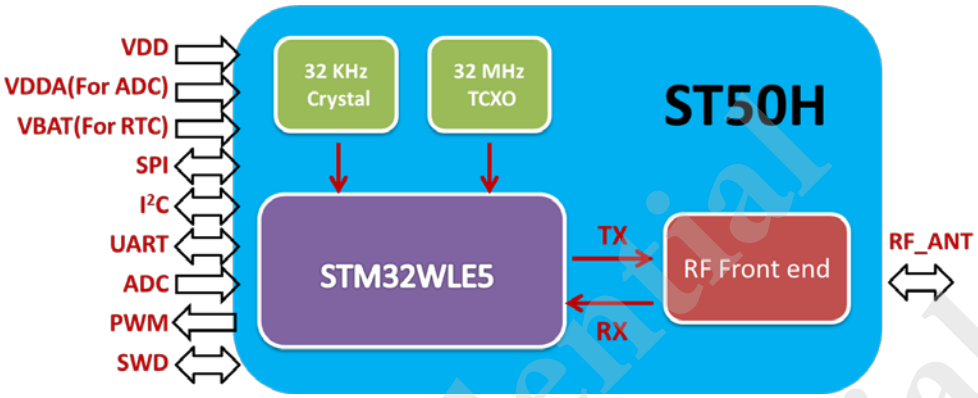


Figure 1, Block Diagram

1-2. Product Version

Part Number	Frequency Range	Spreading Factor	Bandwidth (KHz)	Effective Bitrate (bps)	Est. Sensitivity (dBm)
ST50H	863 – 930 MHz	5 - 12	7.8 - 500	LoRa BR : 0.013 – 17.4 kb/s (G)FSK BR : 0.6 - 300 kb/s	-138 @125kHz, SF12

1-3. Specification

Model Name	ST50H
Product Description	LoRa Wireless Communication Module
Host Interface	UART
Operation Conditions	
Temperature	■ Storage：-50℃ ~ +125℃ ■ Operating：-40℃ ~ +85℃ ■ Low Power Dissipation : -40℃ ~ +95℃ (*Note)
Humidity	■ Operating：10 ~ 95% (Non-Condensing) ■ Storage：5 ~ 95% (Non-Condensing)
Dimension	12 mm x 12 mm x 1.22 mm(Typ.)
Package	LGA73 type

*Note: Low Power Dissipation: means low TX duty cycle and low GPIO driving and sinking current

2. Electrical Characteristics

2-1. Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Standard operating voltage	-0.3		3.9	V
V_{IN}	Input voltage on digital pins	-0.3		3.9	V
Pmr	RF Input Level			+10	dBm

2-2. Recommended Operating Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Standard operating voltage		1.8	3.3	3.6	V
VDDA	Analog supply voltage	ADC or COMP used	1.71		3.6	
		VREFBUF used	2.4			
		ADC, COMP, REFBUF not used	0			
VBAT	Backup operating voltage		1.55		3.6	
VDDSMPS	Power supply for the SMPS step-down converter		1.8		3.6	
VDDRF	Minimum RF voltage		1.8		3.6	
VDDPA	Power supply for power amplifier		1.8		3.6	
VREF+	Positive reference voltage	VDDA ≥ 2 V	2		VDDA	
		VDDA < 2 V	VDDA			
ML	RF Input Level				+10	dBm

2-3. Power Consumption Characteristics

2-3-1. ST50H Power supply scheme

The devices embed two different regulators: one LDO and one DC/DC (SMPS). The SMPS can be optionally switched-on by software to improve the power efficiency. As LDO and SMPS operate in parallel, the SMPS switch-on is transparent to the user and only the power efficiency is affected.

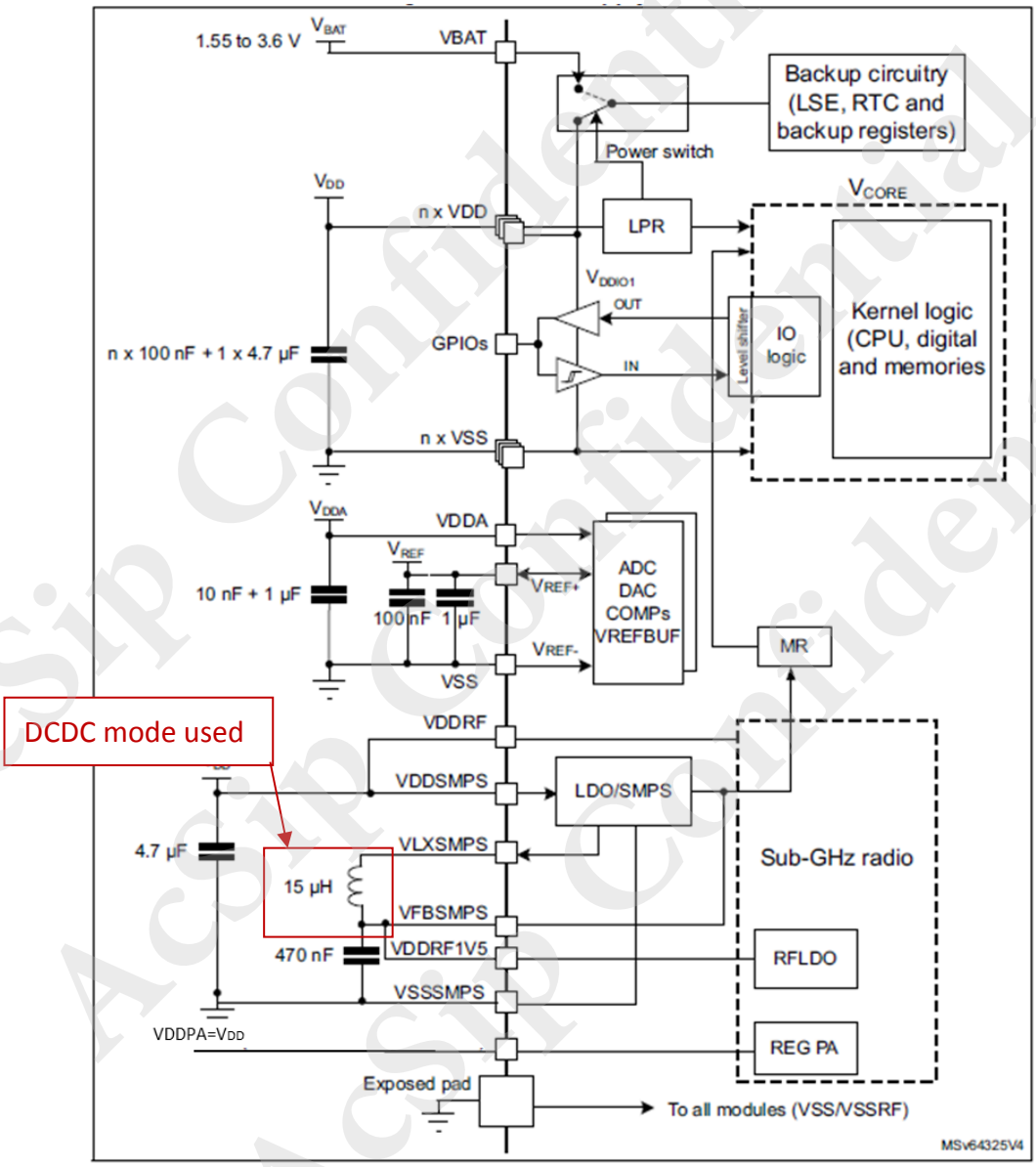


Figure 2, ST50H Power supply scheme

Note: Use of the SMPS is optional. When SMPS is not used (LDO mode), the BOM can be reduced by removing the coil between VLXSMPS and VFBSMPS pins. But it will increase the current consumption.

2-3-2. Current consumption measurement scheme

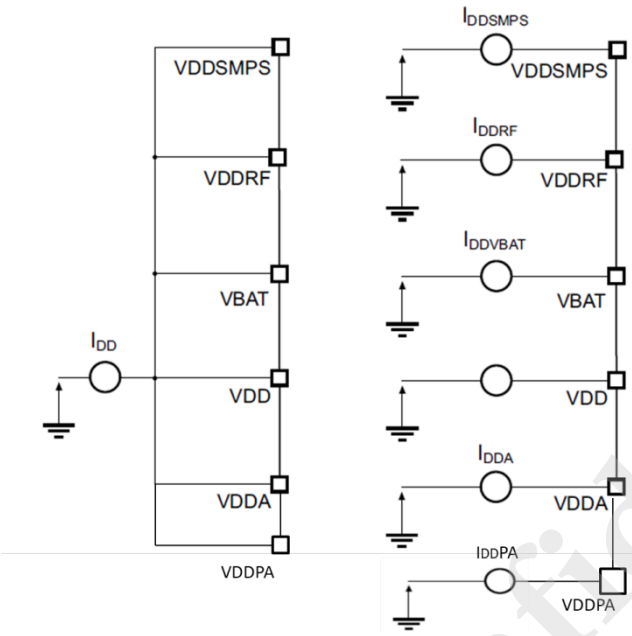


Figure 3, Current consumption measurement scheme

2-3-3. The current consumption

VDD = 3.3 V. The current consumption is measured as described in *Figure 3*. IDD includes current consumption of all supplies (VDDRF, VDDSMPS, VDD, VDDA, VBAT and VDDPA).

Symbol	Parameter	Conditions	Typ.	Max	Unit
IDDSL	Supply current in Sleep mode(Stop 2)		1.3		uA
IDDR	Supply current in Receive mode(SMPS mode used) (SMPS 40 mA max)	RX boosted, LoRa 125 KHz	6.8		mA
IDDT	Supply current in transmit mode with impedance matching(SMPS on) (SMPS 40 mA max) 863~930MHz	RF SetPW = 22dBm RF SetPW = 20dBm RF SetPW = 18dBm RF SetPW = 16 dBm	125 115 110 105		mA

2-4. RF Characteristics

2-4-1. Electrical Specifications

The table below gives the electrical specifications for the transceiver operating with LoRa modulation. Following conditions apply unless otherwise specified:

- VDD = 3.3 V
- Temperature = 25 °C
- FRF = 863 / 915 MHz
- RF impedances matched
- Transmit mode output power defined into a 50 ohm load impedance
- FSK BER = 0.1%, 2-level FSK modulation without pre-filtering, BR = 4.8 kb/s, FDA = ± 5 kHz, BW_F = 20 kHz double-sided
- LoRa® PER = 1%, packet 64 bytes, preamble 8 symbols, CR = 4/5, CRC on payload enabled

2-4-2. Receive Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
RXS_2FB	Sensitivity 2-FSK, RX boosted gain, split RF paths for RX and Tx,RF switch insertion loss excluded	BR=0.6Kbit/s, FDA=0.8 kHz, BW=4 kHz	-	–125	-	dBm
		BR=1.2Kbit/s, FDA=5 kHz, BW=20 kHz	-	–123	-	
		BR=4.8Kbit/s, FDA=5 kHz, BW=20 kHz	-	–117	-	
		BR=38.4bit/s,FDA=40kHz, BW=160 kHz	-	–108	-	
		BR=250Kbit/s,FDA=125kHz,BW=500 kHz	-	–103	-	
RXS_LB	Sensitivity LoRa, RX boosted gain, split RF paths for RX and Tx, RF switch insertion loss excluded	BW = 10.4 kHz, SF = 7	-	–135	-	
		BW = 10.4 kHz, SF = 12	-	–148	-	
		BW = 125 kHz, SF = 7	-	–125	-	
		BW = 125 kHz, SF = 12	-	–138	-	
		BW = 250 kHz, SF = 7	-	–122	-	
		BW = 250 kHz, SF = 12	-	–135	-	
		BW = 500 kHz, SF = 7	-	–118	-	
		BW = 500 kHz, SF = 12	-	–130	-	
RSX_2F	Sensitivity 2-FSK, RX power saving gain with direct tie connection between RX and Tx	BR=4.8 Kbit/s, FDA=5 kHz, BW=20 kHz	-	–115	-	

RXS_L	Sensitivity LoRa, RX power saving gain with direct tie connection between RX and Tx	BW = 125 kHz, SF = 12	-	–135	-	
CCR_F	Co-channel rejection, FSK	-	-	–9	-	dB
CCR_L	Co-channel rejection, LoRa	SF = 7	-	7	-	
		SF = 12	-	19	-	
ACR_F	Adjacent channel rejection, FSK	Offset = ±50 kHz	-	44	-	
ACR_L	Adjacent channel rejection, LoRa	Offset = ±1.5 x BW_L, BW = 125 kHz, SF = 7	-	60	-	
		Offset = ±1.5 x BW_L, BW = 125 kHz, SF = 12	-	71	-	
BI_F	Blocking immunity, FSK	Offset = ±1 MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	67	-	
		Offset = ±2 MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	70	-	
		Offset = ±10 MHz, BR = 4.8 Kbit/s, FDA = 5 kHz, BW = 20 kHz	-	76	-	
BI_L	Blocking immunity, LoRa	Offset = ±1 MHz, BW = 125 kHz, SF = 12	-	87	-	dB
		Offset = ±2 MHz, BW = 125 kHz, SF = 12	-	91	-	
		Offset = ±10 MHz, BW = 125 kHz, SF = 12	-	96	-	
IIP3	Third order input intercept point	Unwanted tones are 1 MHz and 1.96 MHz above LO. 868 to 915 MHz band	-	–9	-	dBm
IMA	Image attenuation	Without IQ calibration	-	30	-	dB
		With IQ calibration	-	54	-	
BW_F	DSB channel filter BW, FSK	Programmable, typical values	4.8	-	467	kHz
TS_RX	Receiver wakeup time	FS to RWX	-	41	-	µs
FERR_L	Maximum tolerated frequency offset Between transmitter and receiver, SF7 to SF12	All bandwidths, ±25 % of BW. The tighter limit between this line and the three lines below applies.	-	±25	-	BW
	Maximumto lerated frequency offset between transmitter and receiver, SF10 to SF12	SF12	–50	-	50	ppm
		SF11	–100	-	100	
		SF10	–200	-	200	

2-4-3. Transmit Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
TXOP	Maximum RF output power	Highest power step setting	20	21	22	dBm
TXDRP	RF output power drop versus supply voltage	RF SetPW =22dBm +22 dBm, VDD = 2.7 V +22 dBm, VDD = 2.4 V +22 dBm, VDD = 1.8 V		2 3 6		dB
TXPRNG	RF output power range	Programmable in 31 step typical value	TXOP-31		TXOP	dBm
TXACC	RF output power step accuracy			± 2		dB
TXRMP	Power amplifier ramping time	Programmable	10	-	3400	µs
TS_TX	Tx wake-up time	Frequency Synthesizer enabled		36 + PA ramping		µs

2-4-4. Digital I/O Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		0.7*VDD		VDD+0.3	V
V_{IL}	Input Low Voltage		-0.3		0.3*VDD	V
V_{IL-N}	Input Low Voltage for pin NRESET		-0.3		0.2*VDD	V
V_{OH}	Output High Voltage	Imax = -2.5 mA	0.9*VDD		VDD	V
V_{OL}	Digital output level low	Imax = 2.5 mA	0		0.1*VDD	V
Ileak	Digital input leakage current (NSS, MOSI, SCK)				1	µA

3. Pin Definition

3-1. Pin Definition

Pin	Definition	I/O	Description
1	PA13	I/O	MCU pin name: PA13
2	PA14	I/O	MCU pin name: PA14
3	VDD	I	VDD
4	VBAT	I	VDD (FOR RTC Power)
5	PC13	I/O	MCU pin name: PC13
6	VREF+	I	Input reference voltage for ADC
7	VDDA	I	External analog power supply for A/D Converters
8	PA15	I/O	MCU pin name: PA15
9	PB15	I/O	MCU pin name: PB15
10	VFBSMPS	I	DC-DC switching power feeback
11	VDDMPS	I	DC-DC switching power input
12	GND	—	Ground pin
13	VLXSMPS	O	DC-DC switching output
14	PB3	I/O	MCU pin name: PB3
15	PB4	I/O	MCU pin name: PB4
16	PB5	I/O	MCU pin name: PB5
17	PB6	I/O	MCU pin name: PB6
18	PB7	I/O	MCU pin name: PB7
19	PB8	I/O	MCU pin name: PB8
20	PB9	I/O	MCU pin name: PB9
21	PC0	I/O	MCU pin name: PC0
22	PC1	I/O	MCU pin name: PC1
23	PC2	I/O	MCU pin name: PC2
24	PC3	I/O	MCU pin name: PC3
25	PC4	I/O	MCU pin name: PC4
26	PC5	I/O	MCU pin name: PC5
27	PC6	I/O	MCU pin name: PC6
28	GND	—	Ground pin
29	PA2	I/O	MCU pin name: PA2
30	PA3	I/O	MCU pin name: PA3

31	PA4	I/O	MCU pin name: PA4
32	PA5	I/O	MCU pin name: PA5
33	PA6	I/O	MCU pin name: PA6
34	PA7	I/O	MCU pin name: PA7
35	GND	—	Ground pin
36	GND	—	Ground pin
37	RF_OUT	I/O	RF_OUT
38	GND	—	Ground pin
39	GND	—	Ground pin
40	NC	—	NC
41	NC	—	NC
42	NC	—	NC
43	Boot 0	I	Boot mode selection pin
44	NRST	I	Hardware reset pin
45	NC	—	NC
46	GND	—	Ground pin
47	GND	—	Ground pin
48	PB11	I/O	MCU pin name: PB11
49	PB10	I/O	MCU pin name: PB10
50	PA9	I/O	MCU pin name: PA9
51	PA8	I/O	MCU pin name: PA8
52	GND	—	Ground pin
53	VDDPA	I	RF PA power input
54	VDDRF	I	RF Segment power input
55	VDD	I	VDD
56	GND	—	Ground pin
57	PB1	I/O	MCU pin name: PB1
58	PB2	I/O	MCU pin name: PB2
59	PB12	I/O	MCU pin name: PB12
60	PB13	I/O	MCU pin name: PB13
61	PB14	I/O	MCU pin name: PB14
62	PA10	I/O	MCU pin name: PA10
63	PA11	I/O	MCU pin name: PA11
64	PA12	I/O	MCU pin name: PA12
65-73	GND	—	Ground pin

3-2. Pin Assignment

The SiP module will conform to the following pin map (top view):

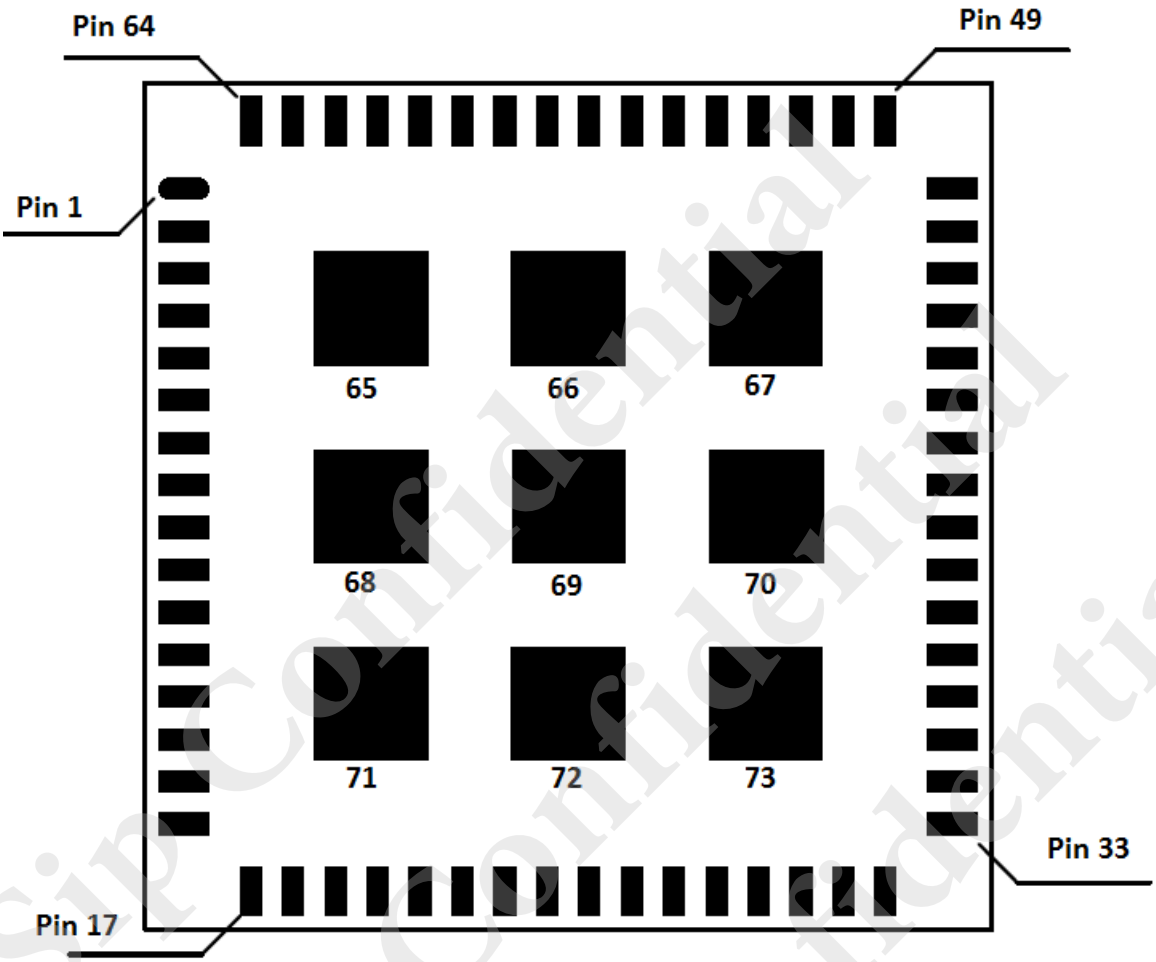


Figure 4, Pin Assignment

3-3. Mechanical Dimension (Typ.)

Unit: mm

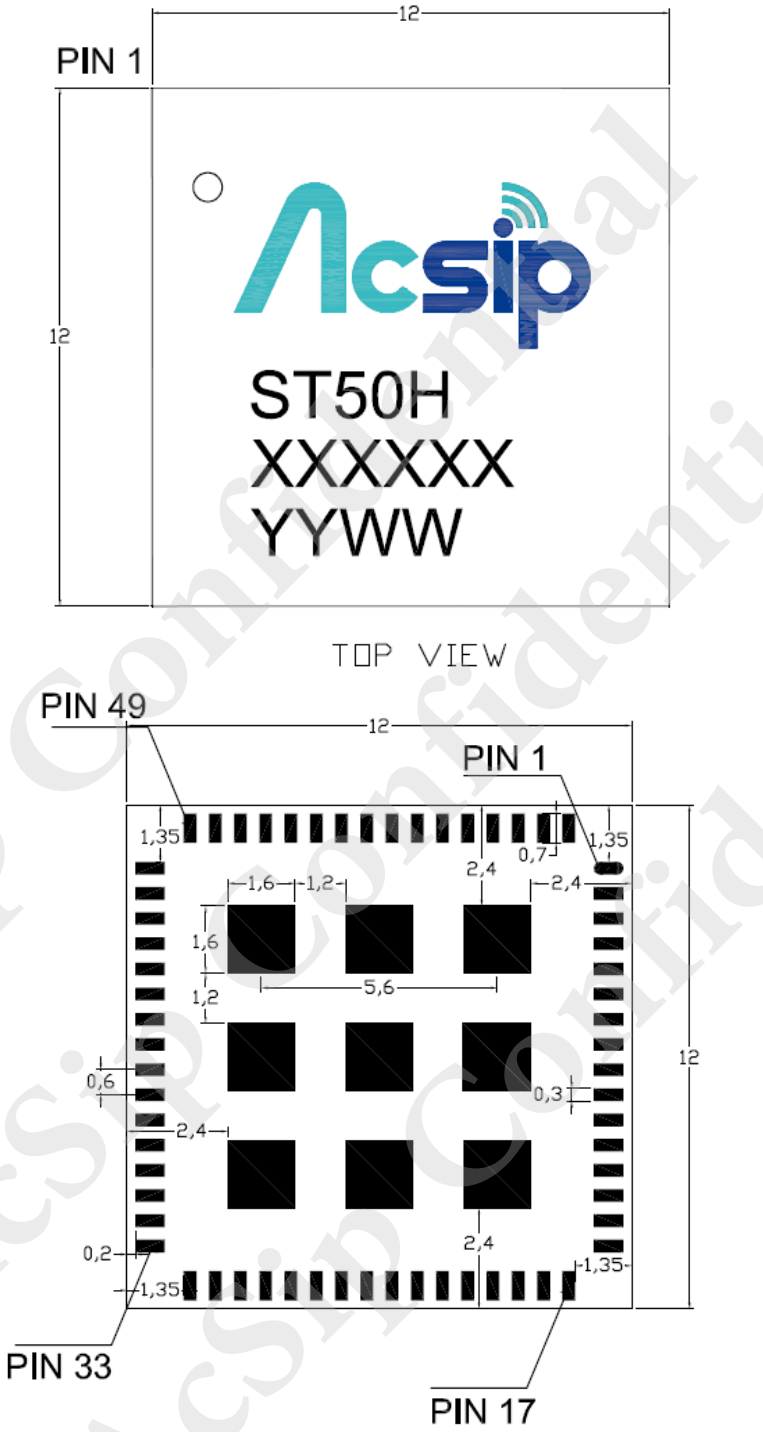


Figure 5, Mechanical Dimension (Typ.)

4. Recommended Footprint

Unit: mm

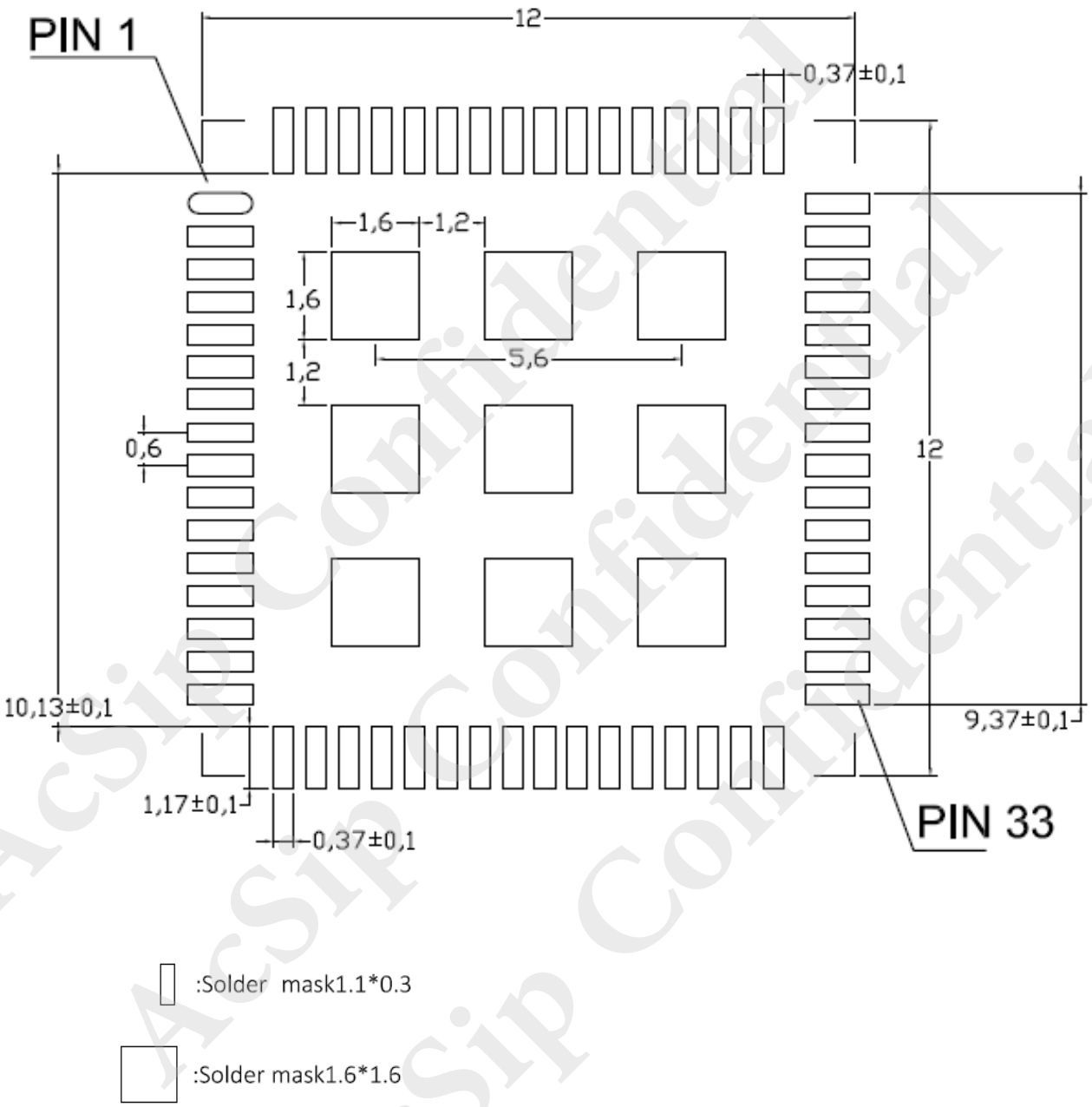
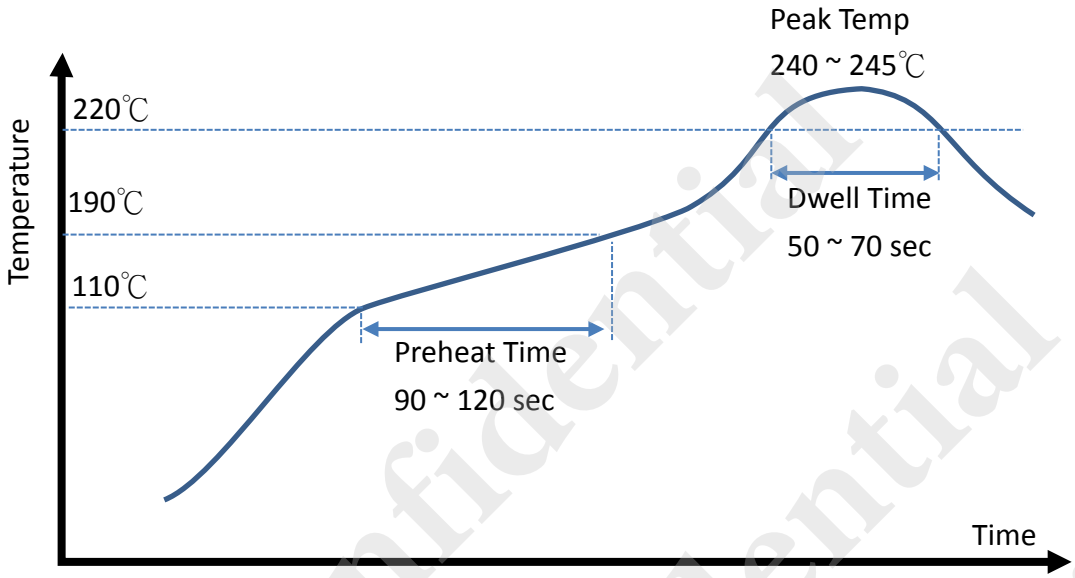


Figure 6, Recommended Footprint

5. Recommended Reflow Profile



Preheat time	110 ~ 190 ℃: 90 ~ 120 sec
Dwell time	above 220 ℃: 50 ~ 70 sec
Peak Temp	240 ~ 245 ℃
Ramp Up/Down Rate	Up : 1~3 ℃/sec Down: 1~5 ℃/sec

The recommended reflow profile is provided as a guideline. Optimal profile may differ due to oven type, assembly layout or other process variables. Nitrogen atmosphere is strongly recommended for best soldering result.

Figure 7, Recommended Reflow Profile

6. SiP Module Preparation

6-1. Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transport and storage with anti -static tray and packing. This protective package must be remained in suitable environment until the module is assembled and soldered onto the main board.

6-2. SMT Preparation

Calculated shelf life in sealed bag: 6 months at<40℃ and <90% relative humidity (RH).

Peak package body temperature: 250℃.

After bag was opened, devices that will be subjected to reflow solder or other high temperature process must.

A. Mounted within: 168 hours of factory conditions<30℃/60%RH.

B. Stored at≦10%RH with N2 flow box.

Devices require baking, before mounting, if:

A. Package bag does not keep in vacuumed while first time open.

B. Humidity Indicator Card is >10% when read at 23±5℃.

C. Expose at 3A condition over 8 hours or Expose at 3B condition over 24 hours.

If baking is required, devices may be baked for 12 hours at 125±5℃.

7.Package Information

7-1. Product Making

Below is the details standard product marking for ST50H.

Cross reference to the applicable line number and table for a full detail of all the variables.

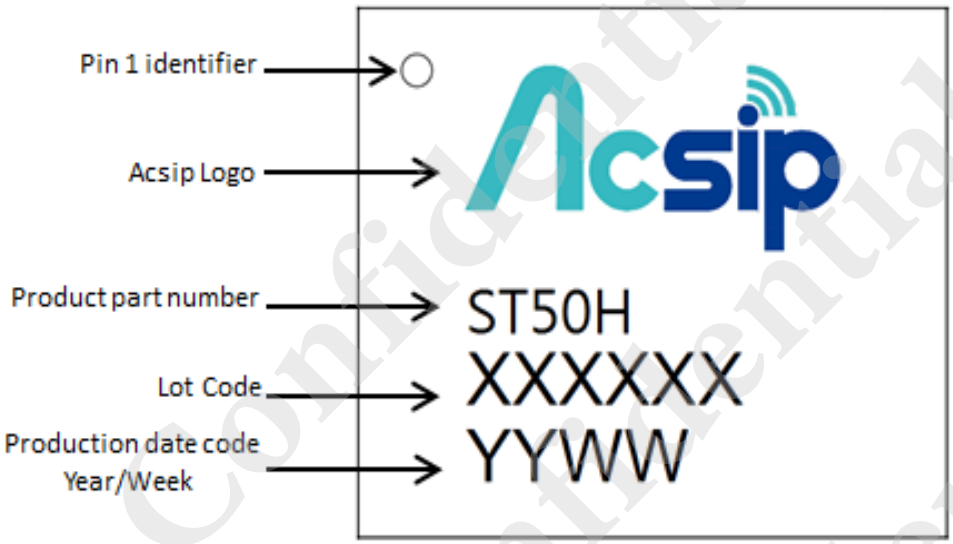
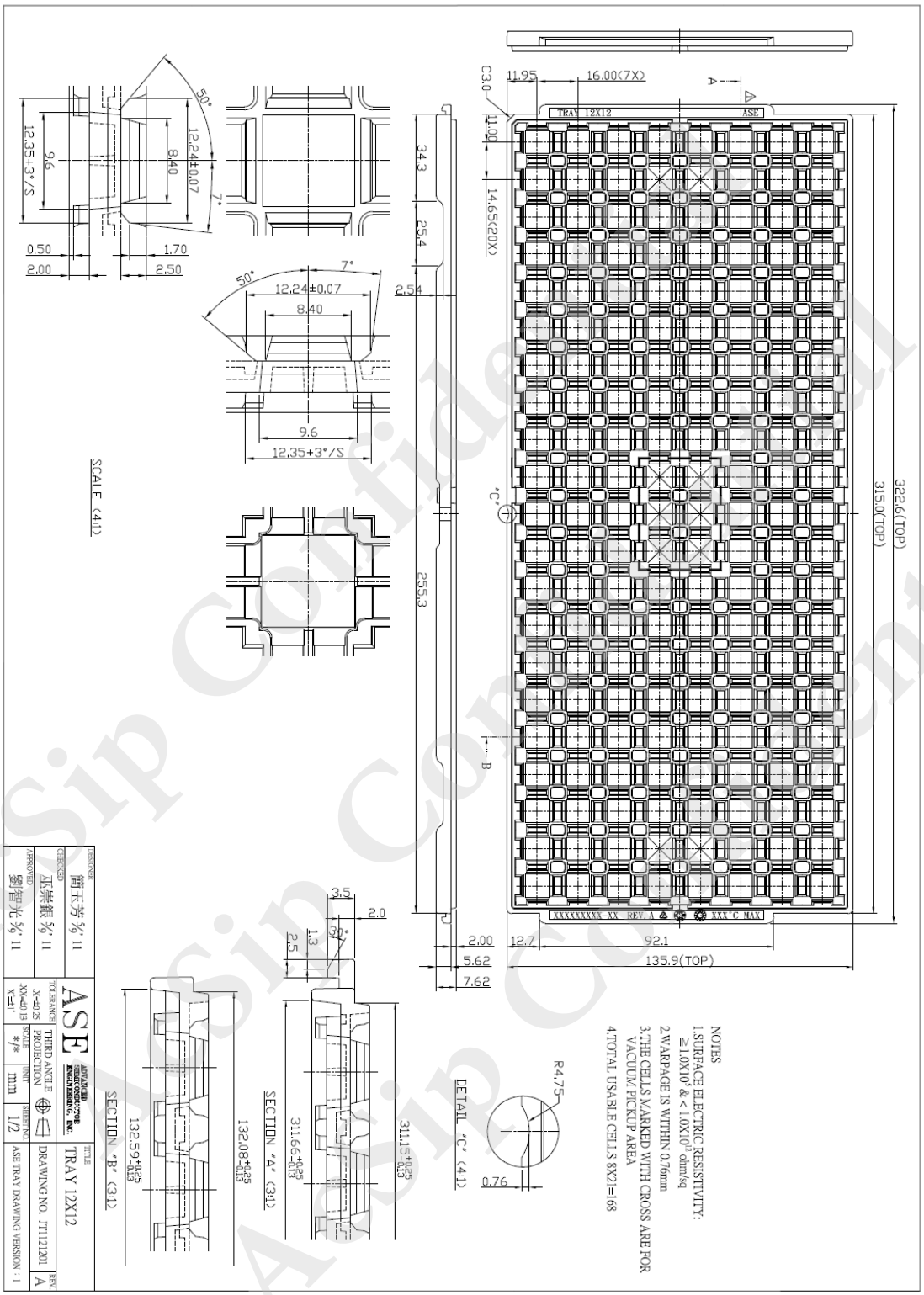
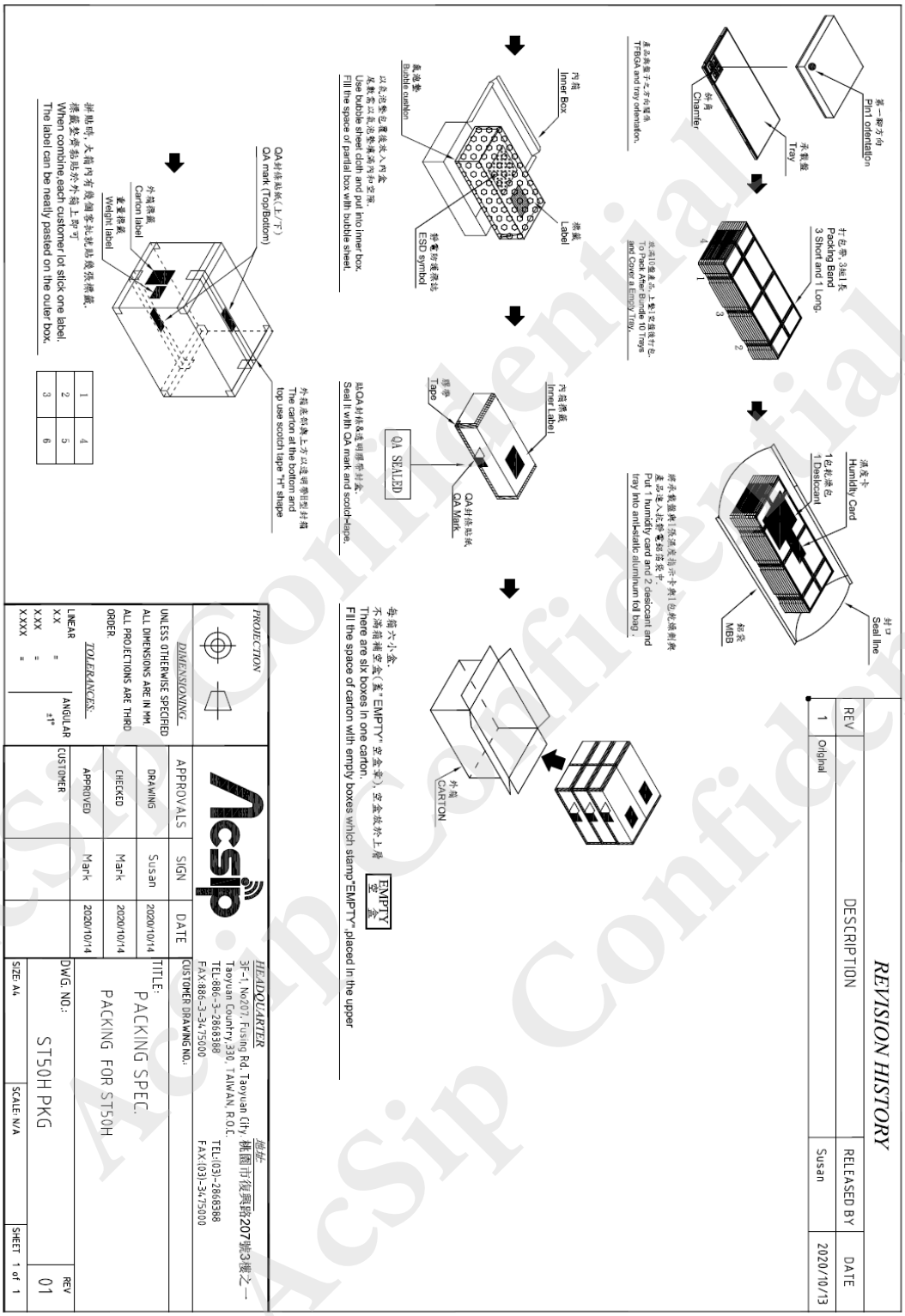


Figure 8, Product Making

7-2. Tray Dimension



7-3. Packing Information



7-4. Humidity Indicator Card

Dry Wet

Indicates 指示點:
10%,20%,30,40%,50%,60% relative humidity
10%,20%,30,40%,50%,60% 相對濕度

Color Change 顏色變化:
Brown (Dry) ---> Blue (Wet)
棕色 (乾燥) ---> 藍色 (潮溼)