EK-AI7933CLD User Guide

Version	H
Doc No	912-13903
Date	2024/12/16

AcSiP Technology Corp
www.acsip.com.tw

Document History

Date	Revised Contents	Revised By	Version
2022/04/29	Initial Version	Ivan	A
2022/08/25	Add FCC Statement	Ivan	B
2022/09/26	Modify Hardware Features	Ivan	C
2022/10/20	Add EVK Schematic	Ivan	D
2022/11/14	Modify Hardware Features	Ivan	E
2024/06/14	Modify EVK Schematic	Ivan	F
2024/08/07	Modify the picture description and pin-header description according to the EVK schematic	Ivan	G
2024/12/16	Add notes for using the SD Card	Ivan	H

INDEX

Lists of Tables and Figures

1. Introduction

1.1 General Description

AI7933CLD is a highly integrated IoT module that features an ARM® Cortex-M33 application processor, a low power 1x1 802.11a/b/g/n/ac/ax dual-band Wi-Fi subsystem, a Bluetooth v5.2 subsystem, an Audio subsystem with Cadence Tensilica HiFi4 processor and a Power Management Unit (PMU). The Wi-Fi subsystem and a Bluetooth v5.2 subsystem offer feature-rich wireless connectivity at high standards, and deliver reliable, cost-effective throughput from an extended distance. The AI7933CLD is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

The AI7933CLD is based on ARM® Cortex-M33 with floating point microcontroller (MCU) including SRAM/ROM memory. The module also supports rich peripheral interfaces, including USB2.0, SDIO, SPI master, I2C, I2S, IR input, UART, AUXADC, PWM, and GPIOs.These features are used to download and debug a project on EK-AI7933CLD.The front view of the EK-AI7933CLD including AI7933CLD module in Figure 1.

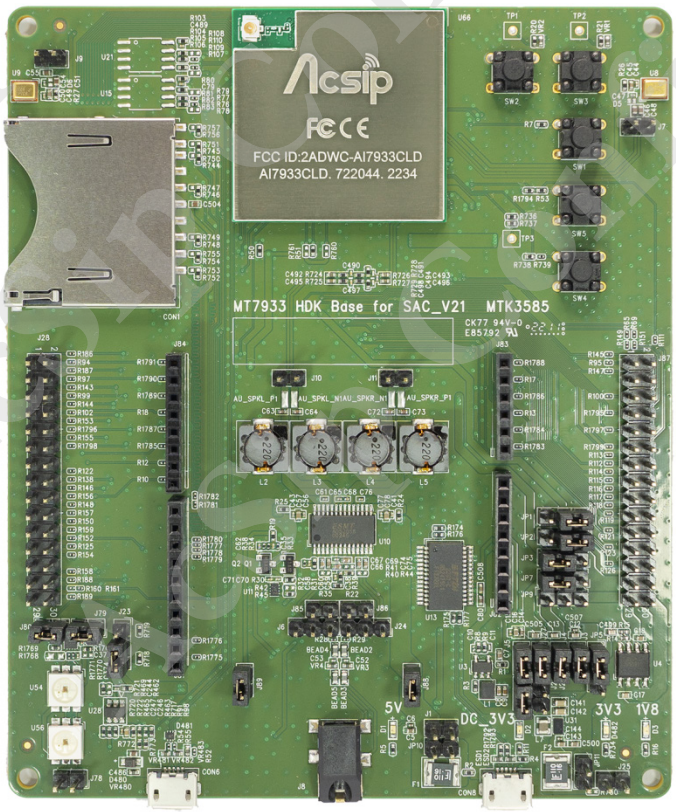


Figure 1. Front view of EK-AI7933CLD

2. Get started with the HDK

Before commencing the application development, you need to configure the development platform.

2.1 Configuring the EK-AI7933CLD

The top view of the EK-AI7933CLD is shown in Figure 2.

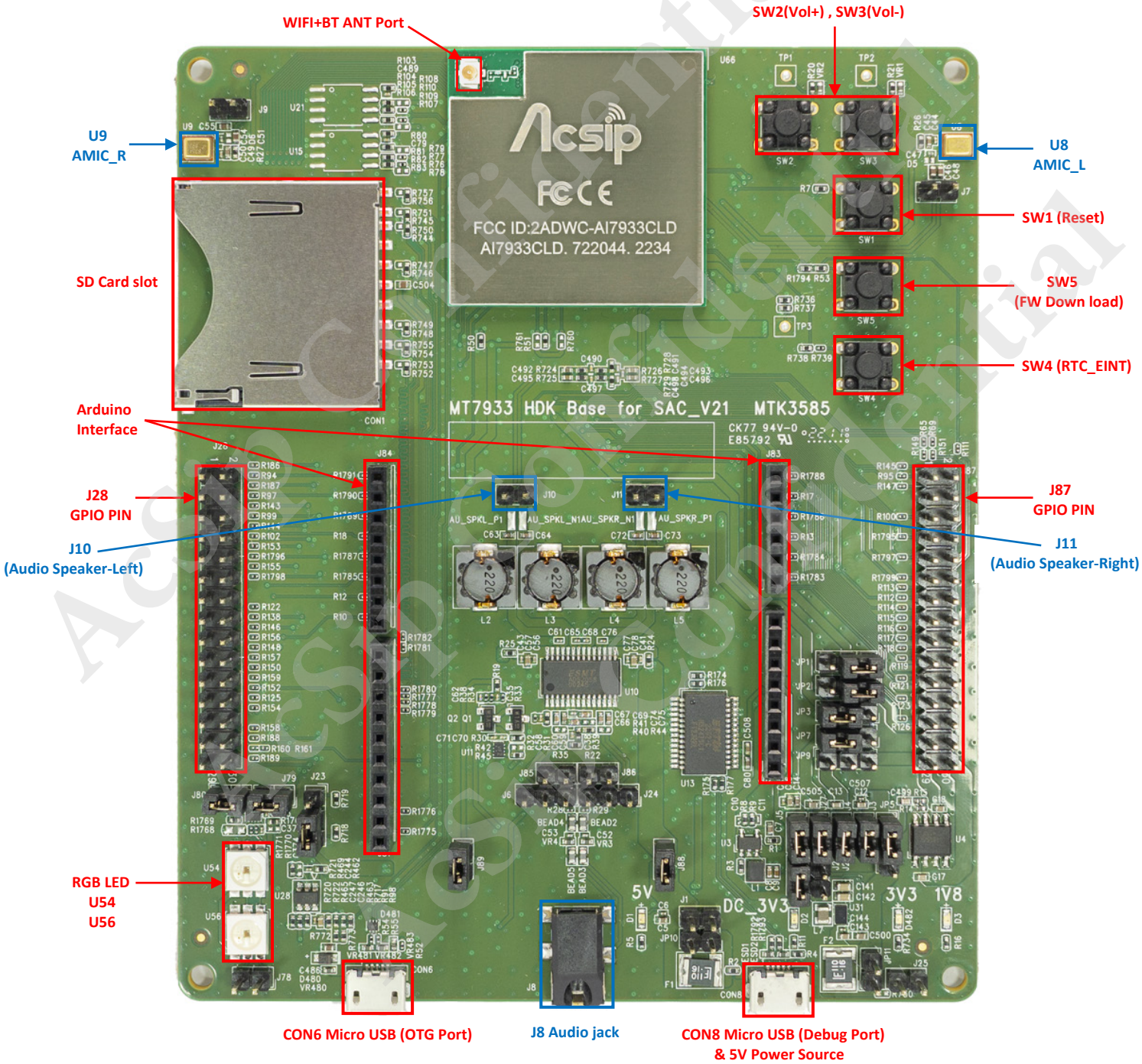


Figure 2. Jumpers and connectors on the EK-AI7933CLD

The description of pins (Figure 2) and their functionality is provided below.

1) CON8 transfer USB interface to UART interface, can debug through UART, transmit, and receive a signal form PC.
2) CON8 is a USB 5V power for EK-AI7933CLD, or you can use external 5V power at J1.
3) CON6 is a USB OTG function com port.
4) Press SW1 to reset the system. For SW2~SW5 more detail, please see “section 4.4”.
5) For Wi-Fi and BT function AI7933CLD module reserve a Wi-Fi + BT IPEX connector. Please connect external antenna to transmit and receive RF signals.
6) U8 and U9 are on-board AMICs which can catch voice command.
7) U54/U56 are RGB LEDs and these RGB LED will be controlled by SPIM interface.
8) J28 and J87 support multifunction GPIO interface, for more detail please refer to “section 4.7”.
9) J10 and J11 is audio speaker pin header which can connect 8ohm/2W speaker to achieve voice assistant function.

2.2 Installing the FTDI drivers on Microsoft Windows

To configure the EK-AI7933CLD:

1) Connect the EK-AI7933CLD CON8 to the computer using a micro-USB cable.
2) Check your PC is x86 or x64 system. And download and install FTDI Windows serial port driver from Here. (The red block showed the download file at below figure)

Currently Supported D2XX Drivers:

		Processor Architecture					
Operating System	Release Date	x86 (32-bit)	x64 (64-bit)	ARM	MIPS	SH4	Comments
Windows*	2017-08-30	2.12.28	2.12.28	-	-	-	WHQL Certified. Includes VCP and D2XX. Available as a setup executable Please read the Release Notes and Installation Guides.
Windows RT	2014-07-04	1.0.2	-	1.0.2	-	-	A guide to support the driver (AN_271) is available here
Linux	2018-06-22	1.4.8	1.4.8	1.4.8 ARMv5 soft-float 1.4.8 ARMv5 soft-float uClibc 1.4.8 ARMv6 hard-float *** 1.4.8 ARMv7 hard-float *** 1.4.8 ARMv8 hard-float ***	1.4.8 MIPS32 soft-float 1.4.8 MIPS32 hard-float 1.4.8 MIPS openwrt-uclibc		If unsure which ARM version to use, compare the output of `readelf` and `file` commands on a system binary with the content of release/build/libftd2xx.txt in each package. ReadMe NEW! Video Install Guide

3) If your OS is Windows7 or 10, please open Windows Control Panel then click System and enter Device Manager.
4) In Device Manager, navigate to Ports (COM & LPT) (see Figure 3).
5) A new COM device should appear under Ports (COM & LPT) in Device Manager, as shown in Figure 3. Note the COMx port number of the serial communication port, this information is needed to send command and receive logs from the COM port.

Due to the com port numbers (COMx) are different at different PC. As red block in Figure 3. showed, means “CM33 UART”.

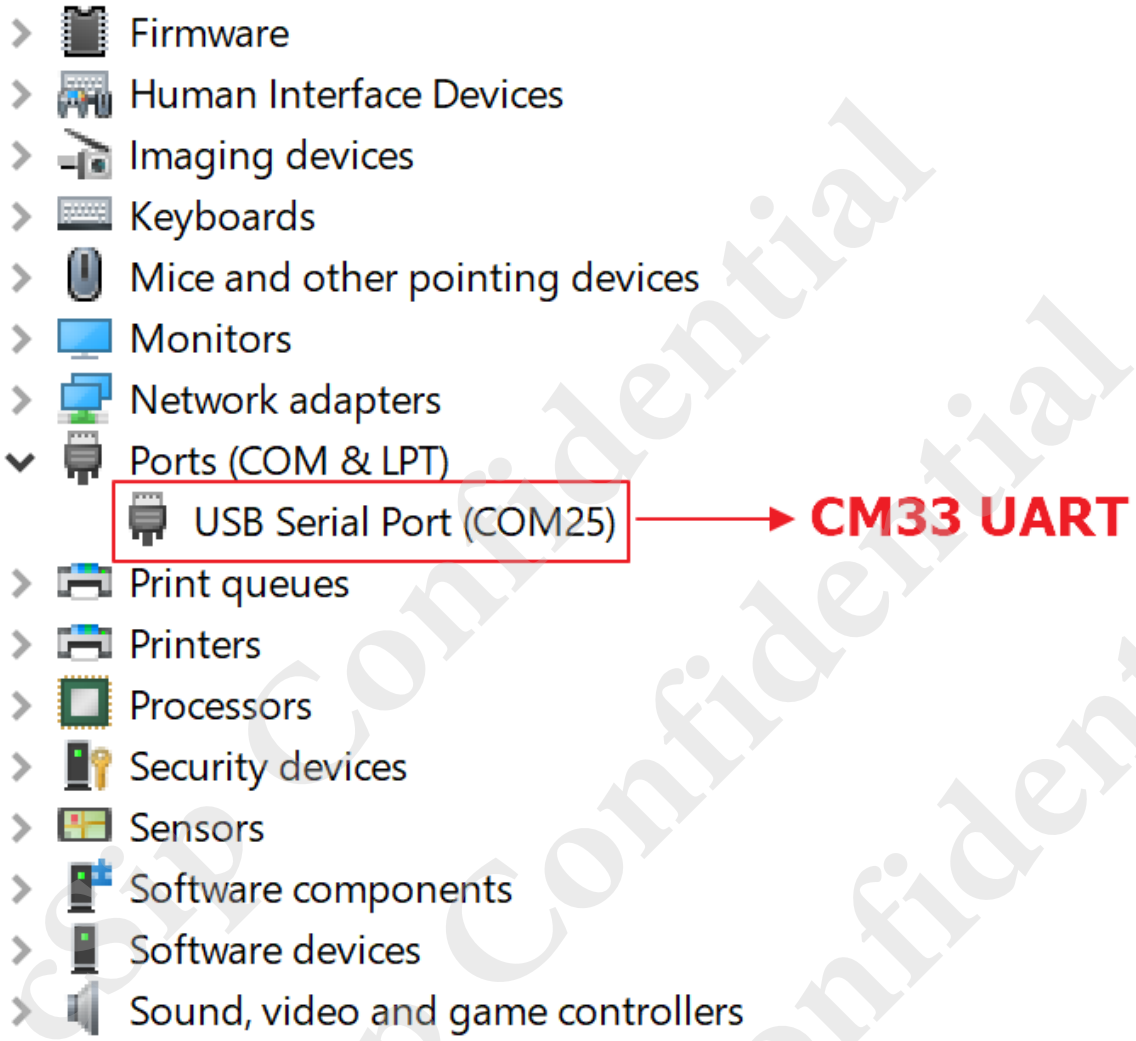


Figure 3. COM port associated with the EK-AI7933CLD

3. Hardware Features

This section provides the main supported features of the EK-AI7933CLD. The detailed description of the features isprovided in the upcoming sections.

3.1 Features Description

3.1.1 Technology and Package

- AI7933CLD LGA-104 module, 32mm X 32mm X 2.7mm (Typ.)

3.1.2 Power Management and Clock Source

- Integrates high efficiency power management unit with single 3.3V power supply input
- Integrates 26MHz crystal clock with low power operation in idle mode
- Integrates 32KHz crystal oscillator or low power sleep mode

3.1.3 Platform

- ARM® Cortex-M33 MCU with FPU with up to 300MHz clock speed
- Embedded 1MB SRAM and 8MB PSRAM
- Embedded 16MB serial flash with eXecute In Place (XIP) and on-the-fly AES
- Supports Hardware crypto engines including AES, DES/3DES, SHA, ECC, TRNG for network security
- Supports up to 46 General Purpose IOs, which are multiplexed with SDIO, SPI, UART, I2C, I2S, AUXADC, PWM and GPIO interfaces
- Supports 12 DMA channels
- Support USB2.0 OTG
- Support RTC Mode

3.1.4 Audio

- Cadence® Tensilica® HiFi4 processor with 600MHz clock speed
- Audio Codec with 3 ADC and 2 DAC channels
- Embedded 256KB SRAM memory for HiFi DSP
- Supports Voice Activity Detection (VAD) and Keyword detection
- On-board headphone jack for external active speaker

3.1.5 Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ac/ax 2.4GHz and 5GHz bands
- Supports 1x1 20MHz bandwidth, MCS0~8(256-QAM) in 2.4G/5GHz band
- Support uplink MU-OFDMA TX and downlink MU-OFDMA RX
- Support Tx LDPC (Low-density parity check)
- Support Rx STBC
- Wi-Fi security WFA WPA/WPA2/WPA3 personal
- QOS supports of WFA WMM
- Support CSI (Channel Signal Information)

3.1.6 Bluetooth

- BT5.2 LE Isochronous Channel
- BT5.1 Advertising Enhancement
- BT5.0 2M_PHY / Long Range / Advertising Extension / SAM / CS#2 / High Duty Cycle Non-Connectable ADV
- BT4.2 Link Layer Privacy / LE Secure Connection / LE Data Packet Length Extension / Link Layer Extended Scanner Filter Policies
- BT4.1 Link Layer Topology / Secure Connection
- BT4.0 and below BR/EDR
- BR/EDR and BLE dual mode concurrent
- Scatternet support: Up to 7 piconets simultaneously with background inquiry/page scan
- Up to 4 BT links + 8 BLE links
- Support SCO and eSCO link with re-transmission
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH
- Supports BT/Wi-Fi coexistence

3.1.7 Miscellaneous

- Embedded eFuse to store specific device information and RF calibration data
- Advanced TDD mode Wi-Fi/Bluetooth coexistence scheme

4. Hardware Feature Configuration

4.1 Microcontroller

The AI7933CLD features an ARM® Cortex-M33 processor, which is the most energy efficient ARM® processor currently available. It supports the clock rates up to 200MHz when core power is 0.7V and 300MHz when core power is 0.8V. The MCU executes the Thump-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication and bit-field manipulation. The AI7933CLD includes a Memory Protection Unit (MPU) in Cortex-M33 MCU to detect unexpected memory access and provides other memory protection features. The AI7933CLD also includes FPU in Cortex-M33 MCU.

4.2 Power Supply

EK-AI7933CLD supports two types of power supply.

1) Power up with a micro-USB connector.

An on-board switching regulator provides voltage of 3.3V for the EK-AI7933CLD, if the power is supplied from an on-board micro-USB connector CON8 (Figure 2). This supply can be isolated from the switching regulator using the jumpers.

Note: that the jumpers J2, J3, J4, J5, J27 pin1 and pin2. JP1, JP2, JP5 pin1 and pin2 are required to be set on. More details on the jumpers can be found in Table 1.

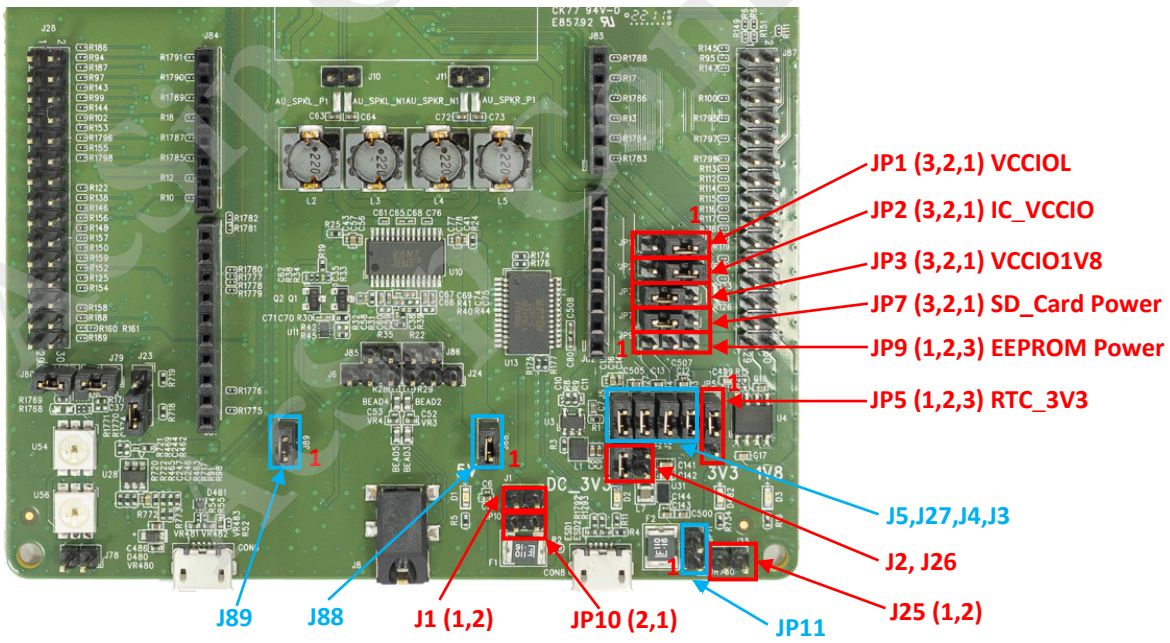


Figure 4. Default power jumper plot

Table 1 Jumper settings for system power input through USB connection

Jumper	Usage	Comments
J1	External 5V power supply	Use external power source to supply 5V voltage to EK-AI7933CLD PCB. Pin 1 is EXUSB_5V, Pin2 is GND.
J2	EXUSB_5V transfer to DC_DC_3V3 power source	Pin 1 is DC_DC_3V3, Pin2 is 3V3_IN. Connect J2 to provide 3.3V power to the system.
J3	AI7933CLD module power source	Pin 1 is 3V3_IN, Pin2 is BASE_3V3. Connect J3 to provide 3.3V power to the AI7933CLD module.
J4	3V3 for EEPROM power	EEPROM has no parts. Pin 1 is 3V3_IN, Pin2 is EXTRA_3V3.
J5	3V3 for level shift IC's power supply	Pin 1 is 3V3_IN, Pin2 is USB_3V3. Convert IC_VCCIO to 3.3V level of SD/FAULT pin of AUDIO_AMP.
J25	External Battery power supply	Pin1 is V_2AA positive endpoint, Pin2 is GND. Use batteries as system power source.
J26	Battery power to 3V3 power source	Pin 1 is V_2AA_O_3V3, Pin2 is 3V3_IN. Connect J26 to power the system from the battery.
J27	3V3 for SD_CARD power	Pin 1 is 3V3_IN, Pin2 is SD_3V3. Connect J27 for power supply
JP1	Switch VCCIO_L to 3V3 power domain or 1V8 power domain	Pin 1 is BASE_3V3, Pin2 is VCCIO_L, Pin3 is VCCIO18. Connect Pin (1,2) or Pin (2,3) to select power domain. Caution: The flash of AI7933CLD default using3V3 power domain, if you want to change VCCIO_L to 1V8 power domain please rework flash to 1V8 power domain flash (eq. W25Q128JWPIQ)
JP2	Switch IC_VCCIO to 3V3 power domain or1V8 power domain	Pin 1 is BASE_3V3, Pin2 is IC_VCCIO, Pin3 is VCCIO18. Connect Pin (1,2) or Pin (2,3) to select power domain.
JP3	Switch VCCIO18 selection Internal or external power supply.	Pin 1 is BASE_1V8, Pin 2 is VCCIO18, Pin 3 is PHYLDO_OUT. Connect Pin (1,2), use external 1.8V power supply. Connect Pin (2,3), use internal 1.8V power supply.
JP5	Switch RTC_3V3 is powered by system 3.3V or battery.	Pin 1 is BASE_3V3, Pin 2 is RTC_3V3, Pin 3 is V_2AA_B_I Connect Pin(1,2), RTC_3v3 is powered by the system(BASE_3V3) Connect Pin(2,3), RTC_3v3 is powered by the battery(V_2AA_B_I)
JP7	Switch SD_Card to 3V3 power domain or 1V8 power domain	Pin 1 is BASE_1V8, Pin 2 is SD_Card VDD, Pin 3 is SD_3V3 Connect Pin(1,2), SD_Card VDD is powered by BASE_1V8 Connect Pin(2,3), SD_Card VDD is powered by SD_3V3
JP9	Switch EEPROM(NC) to 3V3 power domain or 1V8 power domain	Pin 1 is EXTRA_3V3, Pin 2 is EEPROM_P, Pin 3 is BASE_1V8 Connect Pin(1,2),EEPROM is powered by EXTRA_3V3 Connect Pin(2,3),EEPROM is powered by BASE_1V8
J88	5V for (U10) Audio AMP power	Pin 1 is EXUSB_5V, Pin 2 is audio AMP power
J89	5V for (U10) Audio AMP using	Pin 1 is EXUSB_5V, Pin 2 is Audio_VCC_5V

2) Power up using a battery.

When using a battery to power the system, J25 (Pin1+, Pin2-) needs to be connected. The battery voltage range should be between 3.6V and 4.2V. When JP5 (Pin2, Pin3) is connected, RTC_3V3 will become battery powered and the LED light will light up. Remove J2 jumper connector and connect J26. The battery power will provide a stable 3.3V power supply to the system through the Buck-Boost converter IC. As shown in Figure 5.

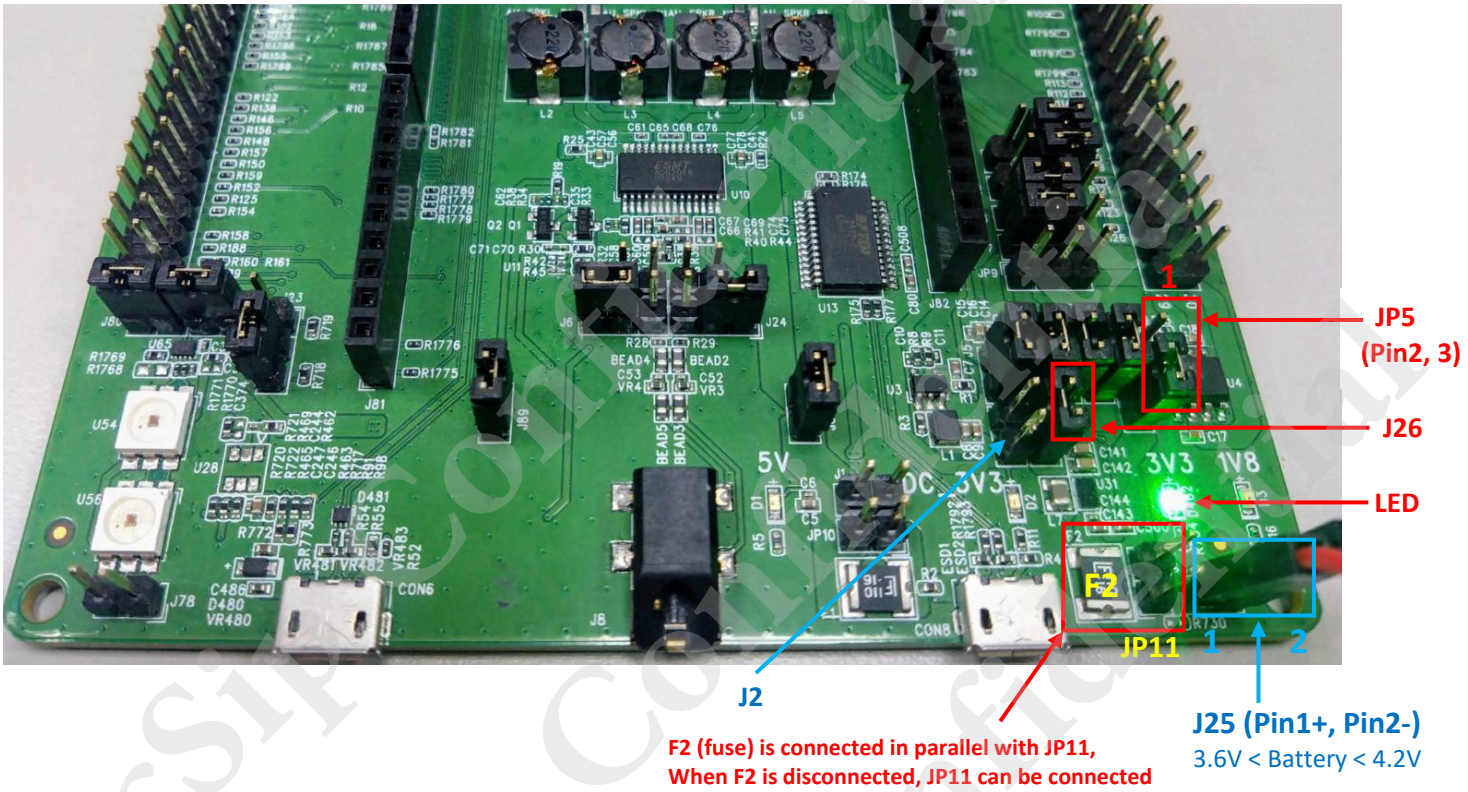


Figure 5. Power up the EK-AI7933CLD using a Battery

4.3 Audio

The EK-AI7933CLD has onboard audio connector associated with different functionalities of the board. The detail of audio related function can refer to Table 2.

Table 2 Audio related function

Item	Detail
J8	3.5mm audio jack for external active speaker.
J6	Audio-Left_P switch, Pin(3,2,1) Pin define (Audio amp_L_in_P, AU_AMP_VOLP, AU_HPL) Connect Pin (2,1) the audio is output by audio jack (J8). Connect Pin(3,2) the audio is output by speaker (J10)
J24	Audio-Right_P switch, Pin(3,2,1) Pin define (AU_HPR, AU_AMP_VORP, Audio amp_R_in_P) Connect Pin (3,2) the audio is output by audio jack (J8). Connect Pin(2,1) the audio is output by speaker (J11)
J85	Audio-Left_N, Pin1 is AU_AMP_VOLN, Pin2 is GND.
J86	Audio-Right_N, Pin1 is GND, Pin2 is AU_AMP_VORN.
J10	Audio header for left speaker, Pin1 is AU_SPKL_P1, Pin2 is AU_SPKL_N1
J11	Audio header for right speaker, Pin1 is AU_SPKR_N1, Pin2 is AU_SPKR_P1
U8	AMIC (AU0_VIN0) for left channel (the microphone hole is set at back side of EK-AI7933CLD)
U9	AMIC (AU0_VIN1) for right channel (the microphone hole is set at back side of EK-AI7933CLD)
SW2	Audio volume up button (KPROW0)
SW3	Audio volume down button (KPROW2)

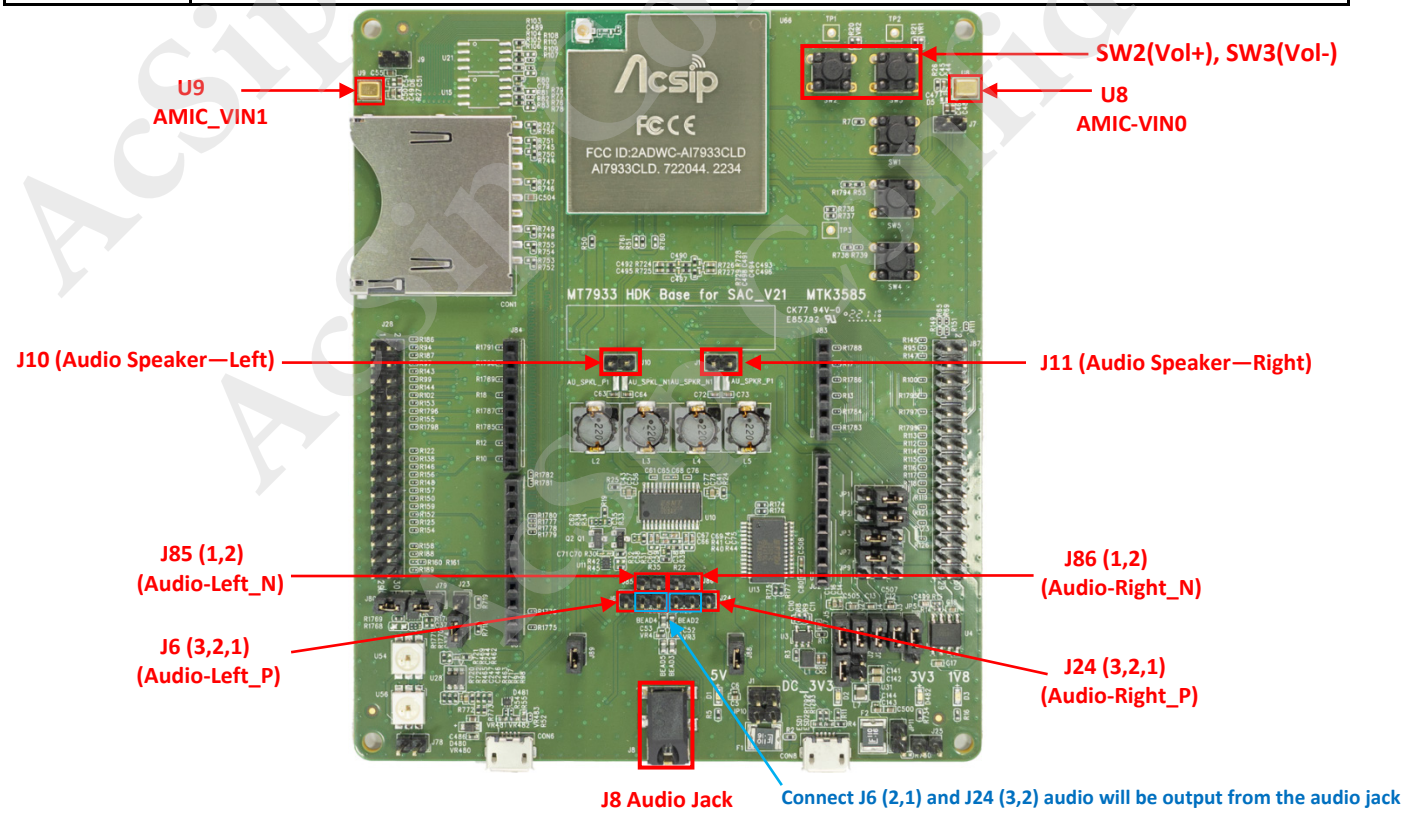


Figure 6 . Audio Jumper and connector Locations

4.4 Buttons

The EK-AI7933CLD is equipped with buttons with the following functionality.

The push buttons are shown in Figure 2. The detail of buttons can refer to Table 3.

Table 3 Buttons

Button	Name	Detail
SW1	SYSRST	Press SW1 to restart the EK-AI7933CLD
SW2	Vol+	Audio volume up button
SW3	Vol-	Audio volume down button
SW4	RTC_EINT	Press SW4 to enable RTC mode
SW5	Force DL mode	Press SW5 to trigger strapping mode (download mode…)

4.5 RGB LED

As Figure7 showed, the EK-AI7933CLD has on-board RGB LEDs (U54/U56) which be controlled by SPIM interface. Please note that ensure jumper J79 and J80 are connected before using RGB LED function. If you want to connect more RGB LEDs, you can connect them through J78

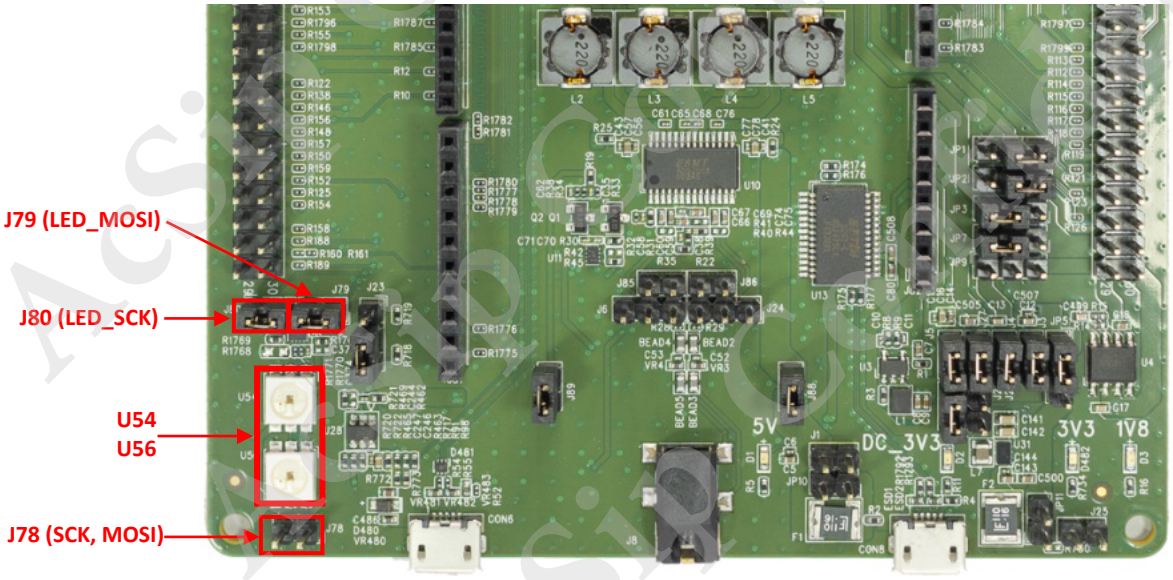


Figure 7. RGB LED

4.6 SD Card

The EK-AI7933CLD has a reserved SD card slot to facilitate users to store data to the SD card. It should be noted that the position of some resistor components needs to be modified before using the SD card. Please refer to figure.8 andswitch R756 to R757; switch R745 to R751; switch R744 to R750; switch R746 to R747; switch R748 to R749; switch R754 to R755; switch R752 to R753.

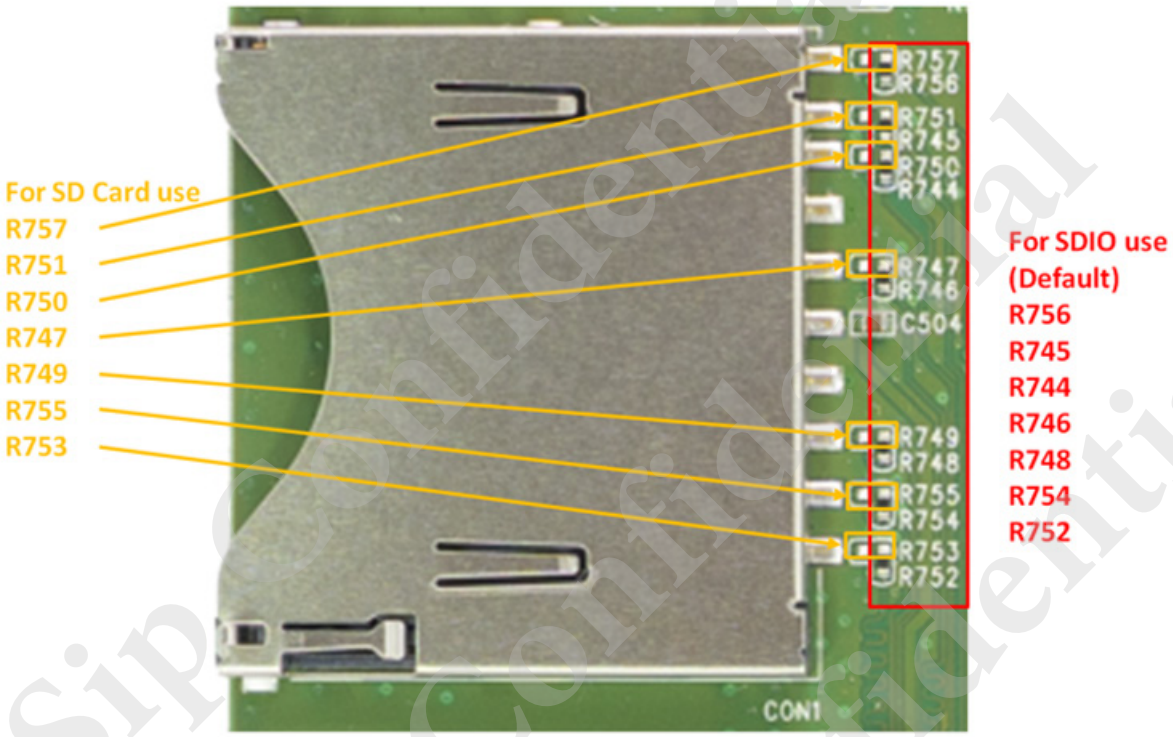


Figure 8. SD card slot rework

Note: AI7933CLD must be powered on before inserting the SD card. If powered on with the SD card inserted, it will cause GPIO_B_0 = 0 and AI7933CLD will not be able to enter normal mode.

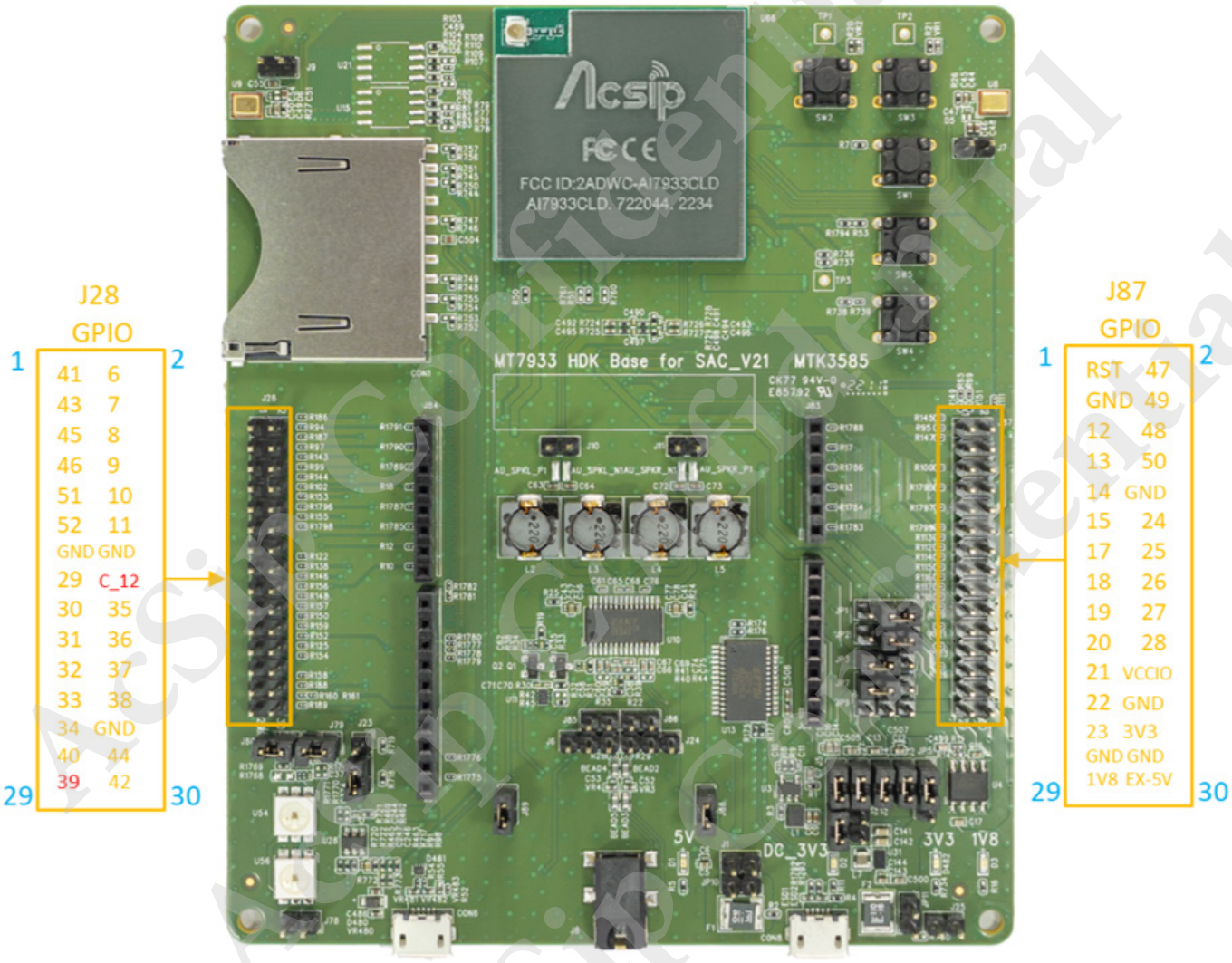
Pin name	Pin description	Pin description	Description
GPIO_B_0	GPIO12	Chip Mode Sel	1: Normal mode: Connect 10kΩ to VCCIO_B 0: RSVD

GPIO_B_0 function in the boot strapping modes

4.7 Extension connectors

The EK-AI7933CLD provides similar pin-out extension connectors for various sensor and device connectivity, as shown in Figure.7 and described in Table 4.

The board has 46 GPIOs multiplexed with other interfaces. Depending on the use case, user can configure each I/O functionality.



Note: GPIO-12 & GPIO-C_12 is the same circuit

GPIO-39 Default to NC

Figure 9. GPIO pin-out extension connectors

Table 4 GPIO pin-out extension connectors

Signal Name	Connector Pin Number	Signal Name	Connector Pin Number
GPIO_0	Reserve for flash	GPIO_27	J87 - 18
GPIO_1	Reserve for flash	GPIO_28	J87 - 20
GPIO_2	Reserve for flash	GPIO_29	J28 - 15
GPIO_3	Reserve for flash	GPIO_30	J28 - 17
GPIO_4	Reserve for flash	GPIO_31	J28 - 19 Reserve for USB OTG
GPIO_5	Reserve for flash	GPIO_32	J28 - 21 Reserve for USB OTG
GPIO_6	J28 - 2 Reserve for Arduino: SPI0_SCK	GPIO_33	J28 - 23 Reserve for USB OTG
GPIO_7	J28 - 4 Reserve for Arduino: SPI0_CSN	GPIO_34	J28 - 25 Reserve for USB OTG
GPIO_8	J28 - 6 Reserve for Arduino: SPI0_MISO	GPIO_35	J28 - 18
GPIO_9	J28 - 8 Reserve for Arduino: SPI0_MOSI	GPIO_36	J28 - 20
GPIO_10	J28 - 10	GPIO_37	J28 - 22
GPIO_11	J28 - 12	GPIO_38	J28 - 24
GPIO_12	J87 - 5	GPIO_39	J28 - 29 Default for AU_AMP_MUTE
GPIO_13	J87 - 7	GPIO_40	J28 - 27
GPIO_14	J87 - 9	GPIO_41	J28 - 1
GPIO_15	J87 - 11	GPIO_42	J28 - 30 Reserve for Arduino: UART1_RX
GPIO_17	J87 - 13	GPIO_43	J28 - 3
GPIO_18	J87 - 15	GPIO_44	J28 - 28 Reserve for Arduino: UART1_TX
GPIO_19	J87 - 17 Reserve for Arduino: I2C1_SDA	GPIO_45	J28 - 5
GPIO_20	J87 - 19 Reserve for Arduino: I2C1_SCL	GPIO_46	J28 - 7
GPIO_21	J87 - 21	GPIO_47	J87 - 2
GPIO_22	J87 - 23	GPIO_48	J87 - 6 Reserve for CM33 UART
GPIO_23	J87 - 25	GPIO_49	J87 - 4
GPIO_24	J87 - 12	GPIO_50	J87 - 8 Reserve for CM33 UART
GPIO_25	J87 - 14	GPIO_51	J28 - 9
GPIO_26	J87 - 16	GPIO_52	J28 - 11

Note: GPIO_39 is AU_AMP_MUTE by default. When using pin headers J28-29pin, resistor R161 needs to be switched to Location of R160.

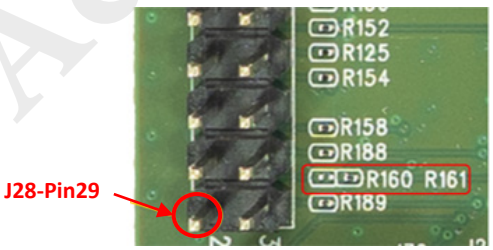


Table 5 GPIO pin multi-function definition

Table 6 GPIO pin multi-function definition

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
PAD_SYSRST_B	NA	PAD_SYSRST_B			PU	Chip hardware fundamental reset pin
SDIO_CLK	0000	GPIO[6]	I/O	I	PD	GPIO 6
	0001*	SDIO_CLK	I			SDIO Clock
	0010	MSDC0_CLK	O			MSDC Clock
	0011	SPIM0_SCK	O			SPI0 (Master) Clock
	0100	CM33_GPIO_EINT0	I			CM33 EINT0
	0101	DEBUG_0	O			Debug Signal 0
	0110	ANT_SEL0	O			Antenna Select 0
	0111	RSVD	I			RSVD
SDIO_CMD	0000	GPIO[7]	I/O	I	PU	GPIO 7
	0001*	SDIO_CMD	I/O			SDIO CMD
	0010	MSDC0_CMD	I/O			MSDC CMD
	0011	SPIM0_CS_N	O			SPI0 (Master) Chip Select
	0100	CM33_GPIO_EINT1	I			CM33 EINT1
	0101	DEBUG_1	O			Debug Signal 1
	0110	ANT_SEL1	O			Antenna Select 1
	0111	RSVD	I			RSVD
SDIO_DAT0	0000	GPIO[8]	I/O	I	PU	GPIO 8
	0001*	SDIO_DAT0	O			SDIO Data[0]
	0010	MSDC0_DAT0	I/O			MSDC0 Data[0]
	0011	SPIM0_MISO	I			SPI0 (Master) Input
	0100	UART0_RTS	O			UART0 RTS
	0101	DEBUG_2	O			Debug Signal 2
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CM33 EINT0
SDIO_DAT1	0000	GPIO[9]	I/O	I	PU	GPIO 9
	0001*	SDIO_DAT1	I/O			SDIO Data[1]
	0010	MSDC0_DAT1	I/O			MSDC0 Data[1]
	0011	SPIM0_MOSI	O			SPI0 (Master) Output
	0100	UART0_CTS	I			UART0 CTS
	0101	DEBUG_3	O			Debug Signal 3
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CM33 EINT1

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
SDIO_DAT2	0000	GPIO[10]	I/O	I	PU	GPIO 10
	0001*	SDIO_DAT2	I/O			SDIO Data[2]
	0010	MSDC0_DAT2	I/O			MSDC0 Data[2]
	0011	I2SIN_DAT0	I			I2S In Data0
	0100	UART0_RX	I			UART0 RX
	0101	DEBUG_4	O			Debug Signal 4
	0110	I2C0_SCL	O			I2C0 Clock
	0111	CM33_GPIO_EINT2	I			CM33 EINT2
SDIO_DAT3	0000	GPIO[11]	I/O	I	PU	GPIO 11
	0001*	SDIO_DAT3	I/O			SDIO Data[3]
	0010	MSDC0_DAT3	I/O			MSDC Data[3]
	0011	I2SO_DAT0	O			I2SO Data
	0100	UART0_TX	O			UART0 TX
	0101	DEBUG_5	O			Debug Signal 5
	0110	I2C0_SDA	I/O			I2C0 Data
	0111	CM33_GPIO_EINT3	I			CM33 EINT3
GPIO_B_0	0000	GPIO[12]	I/O	O	PU	GPIO 12
	0001*	CONN_BGF_UART0_TXD	O			BT General UART TX
	0010	MSDC0_RST	O			MSDC0 Reset
	0011	CONN_BT_TXD	O			BT Debug UART TX
	0100	WIFI_TXD	O			Wi-Fi Debug UART TX
	0101	DEBUG_6	O			Debug Signal 6
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT4	I			CM33 EINT4
GPIO_B_1	0000	GPIO[13]	I/O	I	PU	GPIO 13
	0001*	USB_IDDIG	I			USB OTG ID Pin
	0010	SPIM1_SCK	O			SPIM1 (Master) Clock
	0011	I2SO_BCK	O			I2SO BCK
	0100	UART1_RX	I			UART1 RX
	0101	DEBUG_7	O			Debug Signal 7
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT5	I			CM33 EINT5

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_2	0000	GPIO[14]	I/O	O	PD	GPIO 14
	0001*	USB_DRV_VBUS	O			USB OTG VBUS
	0010	SPIM1_MOSI	O			SPI1 (Master) Output
	0011	I2SO_LRCK	O			I2SO LRCK
	0100	RSVD				RSVD
	0101	DEBUG_8	O			Debug Signal 8
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT6	I			CM33 EINT6
GPIO_B_3	0000	GPIO[15]	I/O	I	PD	GPIO 15
	0001*	USB_OC	I			USB Host Mode Over-Current Input Notify
	0010	SPIM1_MISO	I			SPI1 (Master) Input
	0011	I2SO_MCK	O			I2STX MCLK
	0100	I2SIN_MCK	O			I2SRX MCK
	0101	DEBUG_9	O			Debug Signal 9
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT7	I			CM33 EINT7
GPIO_B_5 (AUXADC)	0000	GPIO[17]	I/O	I	PU	GPIO 17
	0001*	CONN_BGF_UART0_RXD	I			BT General UART RX
	0010	UART0_RX	I			UART0 RX
	0011	TDMIN_MCLK	I			TDMIN MCLK
	0100	DMIC_CLK0	O			DMIC CLK0
	0101	DEBUG_11	O			Debug Signal 11
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT9	I			CM33 EINT9
GPIO_B_6 (AUXADC)	0000	GPIO[18]	I/O	O	PU	GPIO 18
	0001*	CONN_BT_TXD	O			BT Debug UART TX
	0010	UART0_TX	O			UART0 TX
	0011	TDMIN_BCK	I			TDMIN BCK
	0100	DMIC_DAT0	I			DMIC DAT0
	0101	UART1_RX	I			UART1 RX
	0110	IR_IN	I			IR RX Input
	0111	CM33_GPIO_EINT10	I			CM33 EINT10

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_7 (AUXADC)	0000	GPIO[19]	I/O	O	PD	GPIO 19
	0001*	WIFI_TXD	O			Wi-Fi Debug UART TX
	0010	UART0_RTS	O			UART0 RTS
	0011	I2C1_SDA	I/O			I2C1 Data
	0100	I2SIN_LRCK	O			I2SIN LRCK
	0101	UART1_TX	O			UART1 TX
	0110	PTA_EXT_IF_FREQ	I			External PTA Frequency
	0111	CM33_GPIO_EINT11	I			CM33 EINT11
GPIO_B_8 (AUXADC)	0000	GPIO[20]	I/O	I	PD	GPIO 20
	0001*	CONN_WF_MCU_AICE_TCKC	I			Wi-Fi N10 SWD
	0010	UART0_CTS	I			UART0 Control
	0011	I2C1_SCL	O			I2C1 Clock
	0100	I2SIN_BCK	O			I2SIN BCK
	0101	DEBUG_12	O			Debug Signal 12
	0110	PTA_EXT_IF_ACT	I			External PTA Active
	0111	CM33_GPIO_EINT12	I			CM33 EINT12
GPIO_B_9 (AUXADC)	0000	GPIO[21]	I/O	I	PU	GPIO 21
	0001*	CONN_WF_MCU_AICE_TMSC	I/O			Wi-Fi N10 SWD
	0010	PTA_EXT_IF_PRI	I/O			External PTA Priority
	0011	TDMIN_LRCK	I/O			TDMIN LRCK
	0100	DMIC_DAT1	I			DMIC DAT1
	0101	DEBUG_13	O			Debug Signal 13
	0110	ANT_SEL9	O			Antenna Select 9
	0111	CM33_GPIO_EINT13	I			CM33 EINT13
GPIO_B_10 (AUXADC)	0000	GPIO[22]	I/O	I	PD	GPIO 22
	0001*	CONN_BGF_MCU_AICE_TCKC	I			BT N10 SWD
	0010	PTA_EXT_IF_WLAN_ACT	O			External PTA WLAN Active
	0011	TDMIN_DI	I			TDMIN DI
	0100	DMIC_DAT2	I			DMIC Data2
	0101	DEBUG_14	O			Debug Signal 14
	0110	ANT_SEL10	O			Antenna Select 10
	0111	CM33_GPIO_EINT14	I			CM33 EINT14

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_11 (AUXADC)	0000	GPIO[23]	I/O	I	PU	GPIO 23
	0001*	CONN_BGF_MCU_AICE_TMSC	I/O			BT N10 SWD
	0010	DSP_URXD0	I			DSP UART RX
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	DMIC_DAT3	I			DMIC Data3
	0101	DEBUG_15	O			Debug Signal 15
	0110	ANT_SEL11	O			Antenna Select 11
	0111	CM33_GPIO_EINT15	I			CM33 EINT15
GPIO_B_12 (AUXADC)	0000	GPIO[24]	I/O	O	PU	GPIO 24
	0001*	ADSP_JTAG_TDO	O			DSP JTAG
	0010	DSP_UTXD0	O			DSP UART TX
	0011	I2C0_SCL	O			I2C0 Clock
	0100	DMIC_CLK1	O			DMIC CLK1
	0101	RSVD	O			RSVD
	0110	ANT_SEL12	O			Antenna Select 12
	0111	CM33_GPIO_EINT16	I			CM33 EINT16
GPIO_B_13	0000	GPIO[25]	I/O	I	PD	GPIO 25
	0001*	ADSP_JTAG_TCK	I			DSP JTAG
	0010	RSVD	I			RSVD
	0011	UART0_RX	I			UART0 RX
	0100	SPIM0_SCK	O			SPIM0 Clock
	0101	RSVD				RSVD
	0110	UART1_RX	I			UART1 RX
	0111	SPIS_SCK	I			SPIS_SCK
GPIO_B_14	0000	GPIO[26]	I/O	I	PU	GPIO 26
	0001*	ADSP_JTAG_TRST	I			DSP JTAG
	0010	CM33_UART_TX	O			CM33 UART TX
	0011	UART0_TX	O			UART0 TX
	0100	SPIM0_CS_N	O			SPIM0 CS
	0101	RSVD				RSVD
	0110	UART1_TX	O			UART1 TX
	0111	SPIS_CS_N	I			SPIS_CS_N

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_15	0000	GPIO[27]	I/O	I	PU	GPIO 27
	0001*	ADSP_JTAG_TDI	I			DSP JTAG
	0010	RSVD	O			RSVD
	0011	UART0_RTS	O			UART0 RTS
	0100	SPIM0_MISO	I			SPIM0 MISO
	0101	RSVD				RSVD
	0110	UART1_RTS	O			UART1 RTS
	0111	SPIS_MOSI	I			SPIS_MOSI
GPIO_B_16	0000	GPIO[28]	I/O	I	PU	GPIO 28
	0001*	ADSP_JTAG_TMS	I			DSP JTAG
	0010	RSVD	I			RSVD
	0011	UART0_CTS	I			UART0 CTS
	0100	SPIM0_MOSI	O			SPIM0 MOSI
	0101	SPIS_MISO	O			SPIS MISO
	0110	UART1_CTS	I			UART1 CTS
	0111	CM33_GPIO_EINT20	I			CM33_GPIO_EINT20
GPIO_R_0	0000	GPIO[29]	I/O	I	PU	GPIO29
	0001*	DSP_URXD0	I			DSP UART RX
	0010	ADSP_JTAG_TDO	O			DSP JTAG
	0011	PWM_0	O			PWM0
	0100	PTA_EXT_IF_PRI	I/O			External PTA Priority
	0101	CONN_WF_MCU_TDO	O			Wi-Fi N10 JTAG
	0110	RSVD	I			RSVD
	0111	CM33_GPIO_EINT21	I			CM33 EINT21
GPIO_R_1	0000	GPIO[30]	I/O	O	PD	GPIO 30
	0001*	DSP_UTXD0	O			DSP UART TX
	0010	ADSP_JTAG_TCK	I			DSP JTAG
	0011	PWM_1	O			PWM 1
	0100	PTA_EXT_IF_WLAN_ACT	O			External PTA WLAN Active
	0101	CONN_WF_MCU_TCK	I			Wi-Fi N10 JTAG
	0110	CM33_RSVD3	I/O			RSVD
	0111	CM33_GPIO_EINT22	I			CM33 EINT22

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_R_2	0000	GPIO[31]	I/O	O	PD	GPIO 31
	0001*	USB_DRV_VBUS	O			USB Host mode VBUS driving
	0010	ADSP_JTAG_TRST	I			DSP JTAG
	0011	PWM_2	O			PWM2
	0100	PTA_EXT_IF_FREQ	I			External PTA Frequency
	0101	CONN_WF_MCU_TDI	I			Wi-Fi N10 JTAG
	0110	CM33_RSVD0	I			RSVD
	0111	CM33_GPIO_EINT23	I			CM33 EINT23
GPIO_R_3	0000	GPIO[32]	I/O	I	PD	GPIO 32
	0001*	USB_OC	I			USB Host Mode Over-Current Input Notify
	0010	ADSP_JTAG_TDI	I			DSP JTAG
	0011	PWM_3	O			PWM 3
	0100	PTA_EXT_IF_ACT	I			External PTA Active
	0101	CONN_WF_MCU_TRSR_B	I			Wi-Fi N10 JTAG
	0110	RSVD	I			RSVD
	0111	CM33_GPIO_EINT24	I			CM33 EINT24
GPIO_R_4	0000	GPIO[33]	I/O	I	PD	GPIO 33
	0001*	USB_VBUS_VALID	I			USB Device Mode VBUS Detect
	0010	ADSP_JTAG_TMS	I			DSP JTAG
	0011	PWM_4	O			PWM 4
	0100	I2C1_SDA	I/O			I2C1 Data
	0101	CONN_WF_MCU_TMS	I			Wi-Fi N10 JTAG
	0110	RSVD	O			RSVD
	0111	CM33_GPIO_EINT25	I			CM33 EINT25
GPIO_R_5	0000	GPIO[34]	I/O	I	PU	GPIO 34
	0001*	USB_IDDIG	I			USB OTG ID Pin
	0010	I2C0_SCL	O			I2C0 Clock
	0011	PWM_5	O			PWM 5
	0100	I2C1_SCL	O			I2C1 Clock
	0101	RSVD	I			RSVD
	0110	DEBUG_0	O			Debug Signal 0
	0111	CM33_GPIO_EINT26	I			CM33 EINT26

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_R_6	0000	GPIO[35]	I/O	O	PD	GPIO 35
	0001*	UART0_TX	O			UART0 TX
	0010	RSVD	O			RSVD
	0011	PWM_6	O			PWM 6
	0100	PWM_2	O			PWM 2
	0101	CONN_BGF_MCU_TDO	O			BT N10 JTAG
	0110	DEBUG_1	O			Debug Signal 1
	0111	CM33_GPIO_EINT27	I			CM33 EINT27
GPIO_R_7	0000*	GPIO[36]	I/O	I	PD	GPIO 36
	0001	DBSYS_NTRST	I			CM33 JTAG
	0010	CM33_UART_CTS	I			CM33 UART CTS
	0011	PWM_7	O			PWM 7
	0100	PWM_3	O			PWM 3
	0101	CONN_BGF_MCU_TCK	I			BT N10 JTAG
	0110	DEBUG_2	O			Debug Signal 2
	0111	CM33_GPIO_EINT28	I			CM33 EINT28
GPIO_R_8	0000*	GPIO[37]	I/O	I	PD	GPIO 37
	0001	DBSYS_SWCLK_TCLK	I			CM33 JTAG
	0010	I2C1_SDA	I/O			I2C1 Data
	0011	PWM_8	O			PWM 8
	0100	I2C0_SDA	I/O			I2C0 Data
	0101	CONN_BGF_MCU_TDI	I			BT N10 JTAG
	0110	DEBUG_3	O			Debug Signal 3
	0111	CM33_GPIO_EINT29	I			CM33 EINT29
GPIO_R_9	0000*	GPIO[38]	I/O	I	PD	GPIO 38
	0001	DBSYS_TDI	I			CM33 JTAG
	0010	CM33_UART_TX	O			CM33 UART TX
	0011	PWM_9	O			PWM 9
	0100	I2C0_SDA	I/O			I2C0 Data
	0101	CONN_BGF_MCU_TRST_B	I			BT N10 JTAG
	0110	I2C1_SCL	O			I2C1 Clock
	0111	CM33_GPIO_EINT30	I			CM33 EINT30

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_R_10	0000*	GPIO[39]	I/O	I	PD	GPIO 39
	0001	DBSYS_SWDIO_TMS	I/O			CM33 JTAG
	0010	I2C0_SDA	I/O			I2C0 Data
	0011	PWM_10	O			PWM 10
	0100	DSP_URXD0	I			DSP UART RX
	0101	CONN_BGF_MCU_TMS	I			BT N10 JTAG
	0110	ANT_SEL0	O			Antenna Select 0
	0111	RSVD	I			RSVD
GPIO_R_11	0000*	GPIO[40]	I/O	O	PU	GPIO 40
	0001	DBSYS_TDO	O			CM33 JTAG
	0010	RSVD	I			RSVD
	0011	PWM_11	O			PWM 11
	0100	DSP_UTXD0	O			DSP UART TX
	0101	UART0_RX	I			UART0 RX
	0110	ANT_SEL1	O			Antenna Select 1
	0111	RSVD	I			RSVD
GPIO_T_0	0000	GPIO[41]	I/O	I	PD	GPIO 41
	0001	RSVD	I			RSVD
	0010*	DBSYS_NTRST	I			CM33 JTAG
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	CONN_BGF_UART0_RXD	I			BT UART RX
	0101	I2C1_SDA	I/O			I2C1 Data
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CM33 EINT0
GPIO_T_1	0000	GPIO[42]	I/O	I	PD	GPIO 42
	0001	RSVD	I			RSVD
	0010*	DBSYS_SWCLK_TCLK	I			CM33_SWD (Default)
	0011	UART1_RX	I			UART1 RX
	0100	UART0_RX	I			UART0 RX
	0101	DSP_URXD0	I			DSP UART RX
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CM33 EINT1

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_T_2	0000	GPIO[43]	I/O	I	PD	GPIO 43
	0001	RSVD	I			RSVD
	0010*	DBSYS_TDI	I			CM33 JTAG
	0011	I2C0_SCL	O			I2C0 Clock
	0100	CONN_BGF_UART0_TXD	O			BT UART TX
	0101	I2C1_SCL	O			I2C1 Clock
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT17	I			CM33 EINT17
GPIO_T_3	0000	GPIO[44]	I/O	I	PD	GPIO 44
	0001	RSVD	I/O			RSVD
	0010*	DBSYS_SWDIO_TMS	I			CM33_SWD (Default)
	0011	UART1_TX	O			UART1 TX
	0100	UART0_TX	O			UART0 TX
	0101	DSP_UTXD0	O			DSP UART TX
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT18	I			CM33 EINT18
GPIO_T_4	0000	GPIO[45]	I/O	O	PU	GPIO 45
	0001	RSVD	O			RSVD
	0010*	DBSYS_TDOO	O			CM33 JTAG
	0011	I2C1_SDA	I/O			I2C1 Data
	0100	WIFI_TXD	O			Wi-Fi Debug UART TX
	0101	PWM_0	O			PWM0
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT19	I			CM33 EINT19
GPIO_T_5	0000	GPIO[46]	I/O	O	PU	GPIO 46
	0001*	SPIM0_SCK	O			SPIM0 SCK
	0010	RSVD	O			RSVD
	0011	I2C1_SCL	O			I2C1 Clock
	0100	CONN_WF_MCU_AICE_TCKC	I			Wi-Fi N10 SWD
	0101	PWM_1	O			PWM 1
	0110	ANT_SEL7	O			Antenna Select 7
	0111	RSVD				RSVD

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
KPROW_0	0000	GPIO[47]	I/O	O	PU	GPIO 47
	0001*	SPIM0_CS_N	O			SPIM0 CS
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPROW_0	I/O			KEYPAD_KPROW_0
	0100	CONN_WF_MCU_AICE_TMSC	I/O			Wi-Fi N10 SWD
	0101	PWM_2	O			PWM 2
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT2	I			CM33 EINT2
KPROW_1	0000	GPIO[48]	I/O	I	PU	GPIO 48
	0001*	CM33_UART_RX	I			CM33 UART RX (default)
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPROW_1	I/O			KEYPAD_KPROW_1
	0100	DSP_URXD0	I			DSP UART RX
	0101	PWM_3	O			PWM 3
	0110	ANT_SEL9	O			Antenna Select 9
	0111	AUDIO_DEBUG_IN_0	I			AUDIO_DEBUG_IN_0
KPROW_2	0000	GPIO[49]	I/O	O	PU	GPIO 49
	0001*	RSVD	O			RSVD
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPROW_2	I/O			KEYPAD_KPROW_2
	0100	CONN_BT_TXD	O			BT Debug UART TX
	0101	PWM_4	O			PWM 4
	0110	ANT_SEL10	O			Antenna Select 10
	0111	AUDIO_DEBUG_IN_1	I			AUDIO_DEBUG_IN_1
KPCOL_0	0000	GPIO[50]	I/O	O	PU	GPIO 50
	0001*	CM33_UART_TX	O			CM33 UART TX (default)
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPCOL_0	I			KEYPAD_KPCOL_0
	0100	DSP_UTXD0	O			DSP UART TX
	0101	PWM_5	O			PWM 5
	0110	ANT_SEL11	O			Antenna Select 11
	0111	AUDIO_DEBUG_IN_2	I			AUDIO_DEBUG_IN_2

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
KPCOL_1	0000	GPIO[51]	I/O	I	PD	GPIO 51
	0001*	SPIM0_MISO	I			SPIM0 MISO
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPCOL_1	I			KEYPAD_KPCOL_1
	0100	CONN_BGF_MCU_AICE_TCKC	I			BT N10 SWD
	0101	PWM_6	O			PWM 6
	0110	ANT_SEL12	O			Antenna Select 12
	0111	AUDIO_DEBUG_IN_3	I			AUDIO_DEBUG_IN_3
KPCOL_2	0000	GPIO[52]	I/O	O	PU	GPIO 52
	0001*	SPIM0_MOSI	O			SPIM0 MOSI
	0010	CM33_UART_RX	I			CM33 UART RX
	0011	KEYPAD_KPCOL_2	I			KEYPAD_KPCOL_2
	0100	CONN_BGF_MCU_AICE_TCKC	I/O			BT N10 SWD
	0101	PWM_7	O			PWM 7
	0110	UART1_TX	O			UART1 TX
	0111	AUDIO_DEBUG_IN_4	I			AUDIO_DEBUG_IN_4

4.8 RTC

The AI7933CLD features a RTC module, clock source operates at 32.768kHz crystal oscillator. RTC has built-in accurate timer to wake up the system when the user-defined timer expires. RTC uses a different power source from the Power Management Unit (PMU). In retention mode, the PMU is turned off while the RTC module remains powered on. The RTC module only consumes 6μA in retention mode.

5. Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Country Code selection feature to be disabled for products marketed to the US/CANA

Integration instructions for host product manufacturers

Applicable FCC rules to module

FCC Part 15.247

FCC Part 15.407

Summarize the specific operational use conditions

The module is must be installed in mobile device.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Limited module procedures

Not applicable

Trace antenna designs

Not applicable

RF exposure considerations

20 cm separation distance and co-located issue shall be met as mentioned in “Summarize the specific operational use conditions”.

Product manufacturer shall provide below text in end-product manual
“This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.”

Antennas

Brand Name	Model Name	Antenna Type	Antenna Gain	Antenna Connector
SINBON	IAHA202205004	PCB Dipole	4.99 dBi	RF Mini Plug
SINBON	IAHA202205005	FPC Dipole	4.36 dBI	RF Mini Plug

Label and Compliance Information

Product manufacturers need to provide a physical or e-label stating
“Contains FCC ID: 2ADWC-AI7933CLD” with finished product

Information on Test Modes and Additional Testing Requirements

Test tool: termite-3.3 shall be used to set the module to transmit continuously.

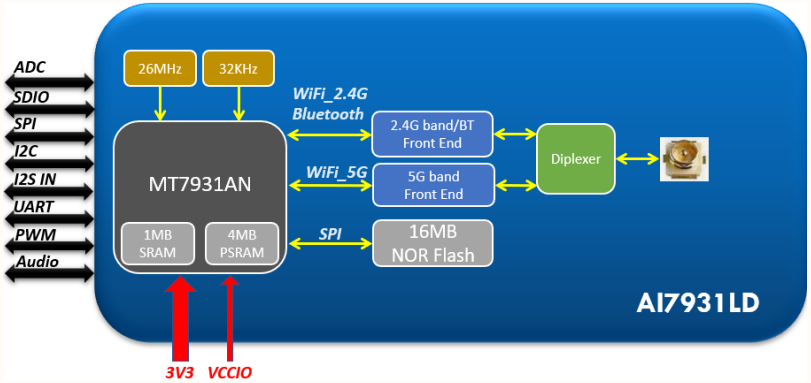
Additional Testing, Part 15 Subpart B Disclaimer

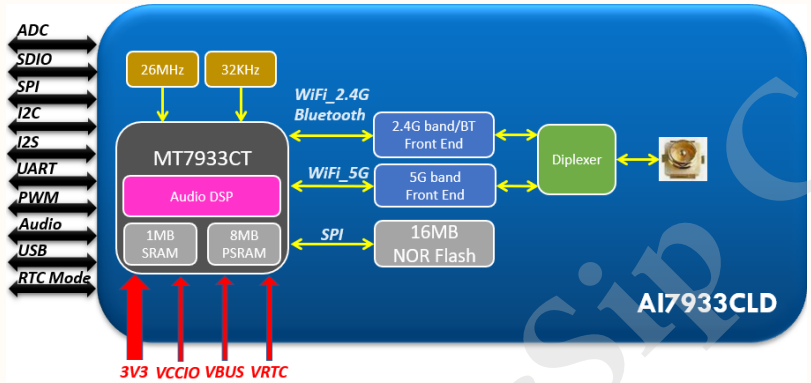
The module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

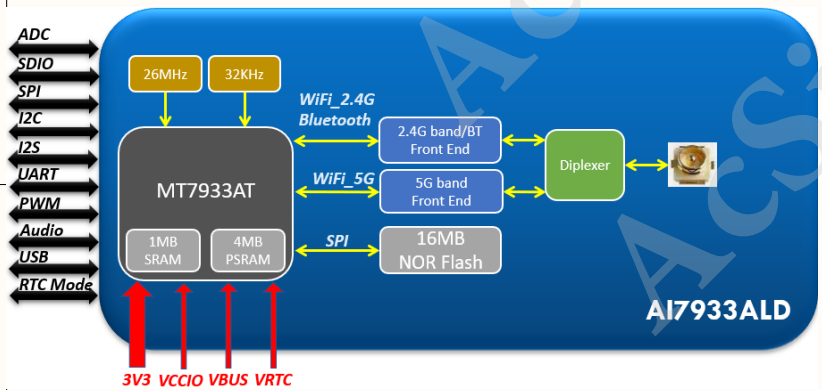
6. EVK Schematic

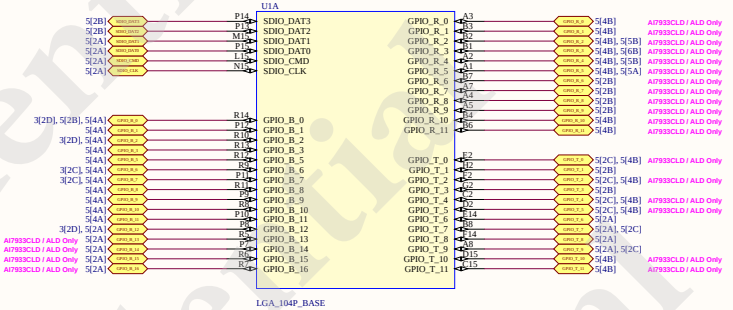
The following figure is the Schematic of EK-AI7933CLD

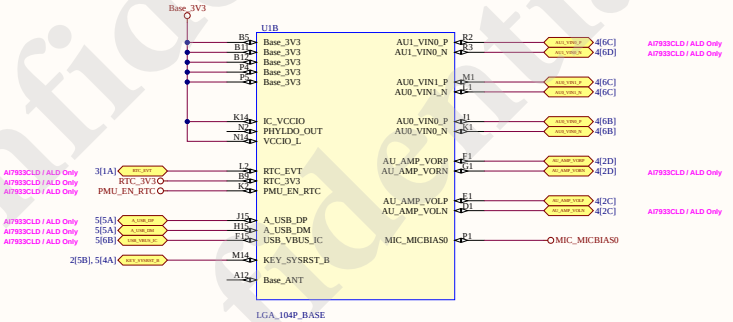
AI7931LD / AI7933CLD / AI7933ALD Module

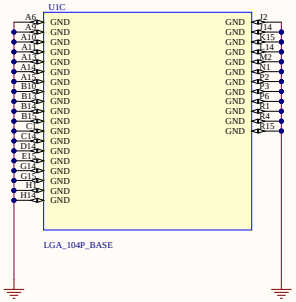




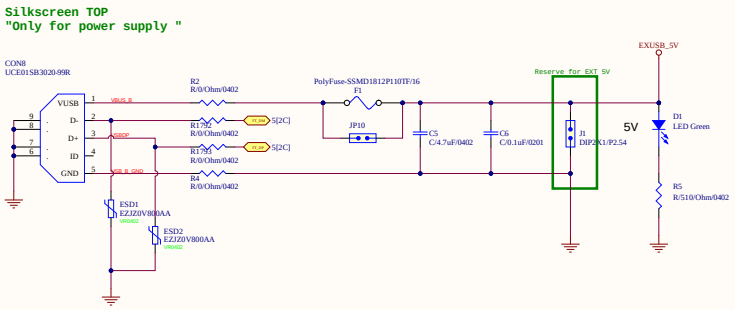




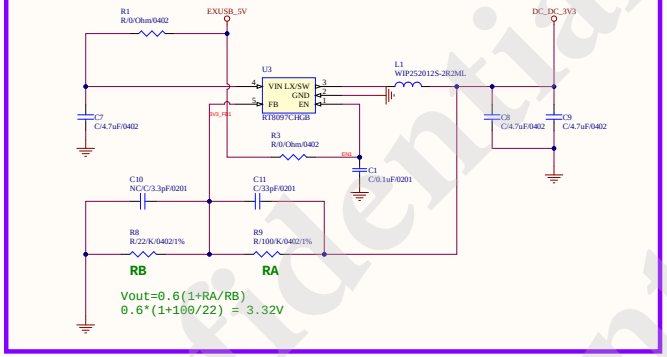




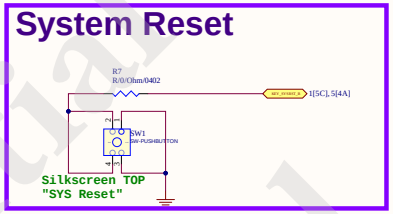
Extra USB 5V Power



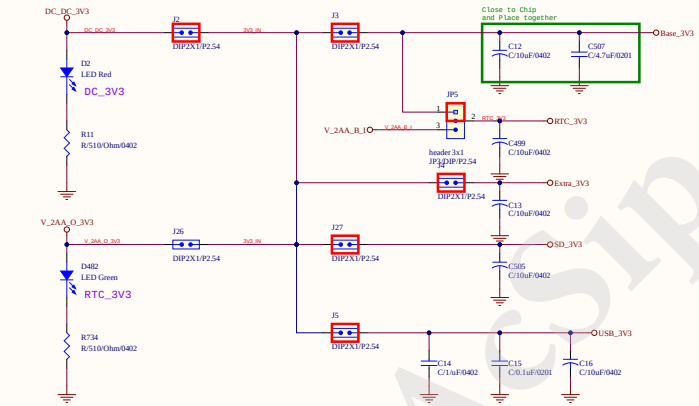
DC to DC 3.3V



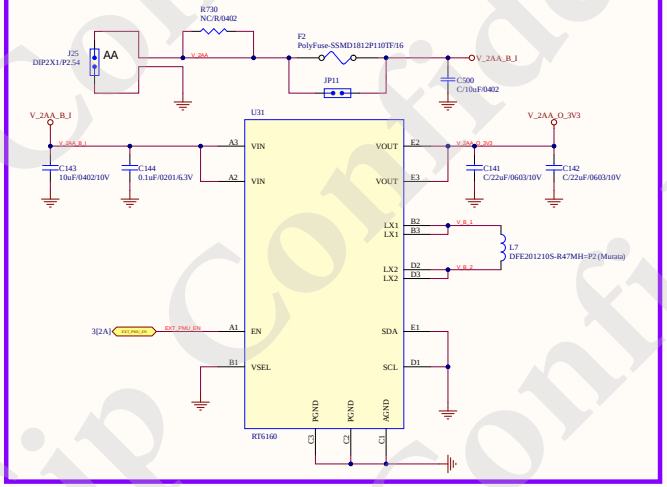
System Reset



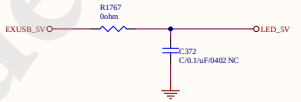
3.3V Power Tree



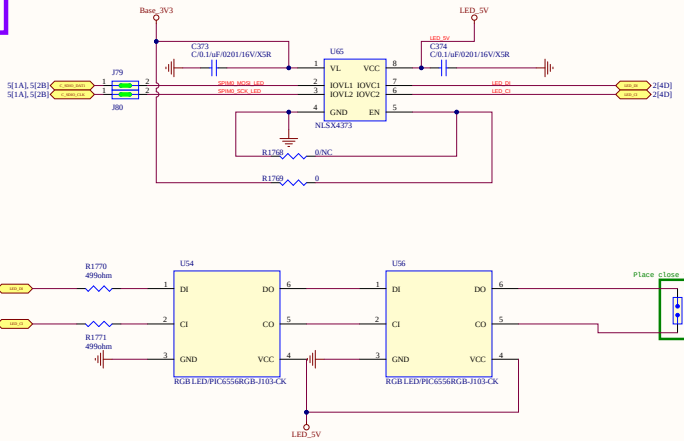
2xAA Battery



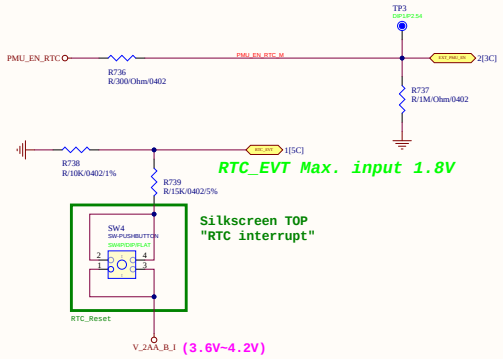
LED Power Plan



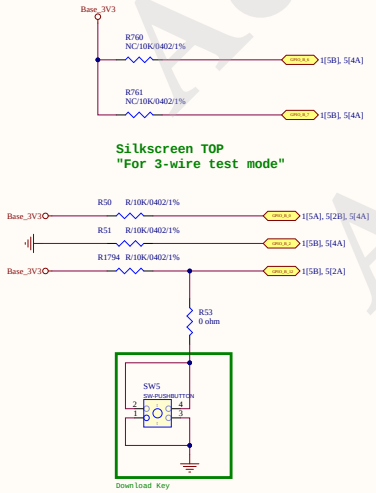
LED Level Shift



RTC Interrupt (AI7933CLD / ALD Only)



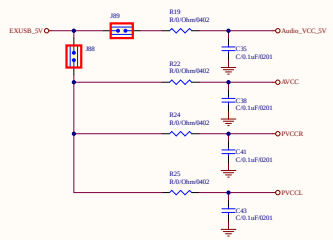
Strap (Mode Selection)



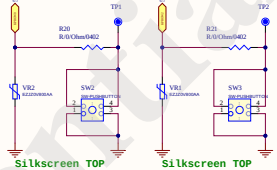
Function	Pin	Sub-Function	Pin	Read-only CR	Value	Description
Normal mode XTEST=0	PAD_GPIO_B_0 = 1	Force DL	{PAD_GPIO_B_2, PAD_GPIO_B_12}	0x30034010[1:0]	00	CM33 UART DL Mode
					01	CM33 Flash normal boot
					10	CM33 SDIO DL Mode
					11	CM33 USB DL Mode
		Xtal mode	PAD_SF_QPI_CS	0x30034010[2]	0	Xtal buffer mode
					1	Xtal normal mode
Test mode XTEST=1	PAD_GPIO_B_0 = 0	test_mode[3:0]	{PAD_GPIO_B_12, PAD_GPIO_B_7, PAD_GPIO_B_6, PAD_GPIO_B_2}	0x30034010[4]	0000	T_Power_ON_DBG_mode
				0x30034010[5]	0001	ATPG mode
				0x30034010[6]	0010	T_FT_mode_pwr_on
				0x30034010[7]	0011	T_FT_mode_pwr_off
				0x30034010[8]	0100	T_SLP
				0x30034010[9]	0101	T_HIF_USB_U2
				0x30034010[10]	0110	T_BT_AFE_ADC
				0x30034010[11]	0111	T_BT_WF_RF
				0x30034010[12]	1000	T_BT_TSSI_ADC
				0x30034010[13]	1001	T_AFE_RXDS
				0x30034010[14]	1010	T_AUD_ADC
				0x30034010[15]	1011	T_AUXADC
				0x30034010[16]	1100	T_NAND_TREE
				0x30034010	1101	T_TESTIF_MCU

Module Audio Part (AI7933CLD Only)

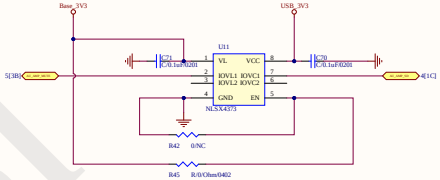
Audio Power Plan



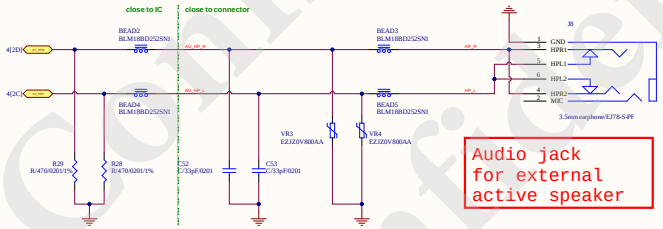
Volumn Key Pad



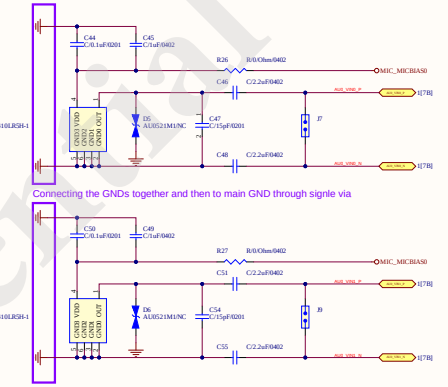
Level Shift Circuit



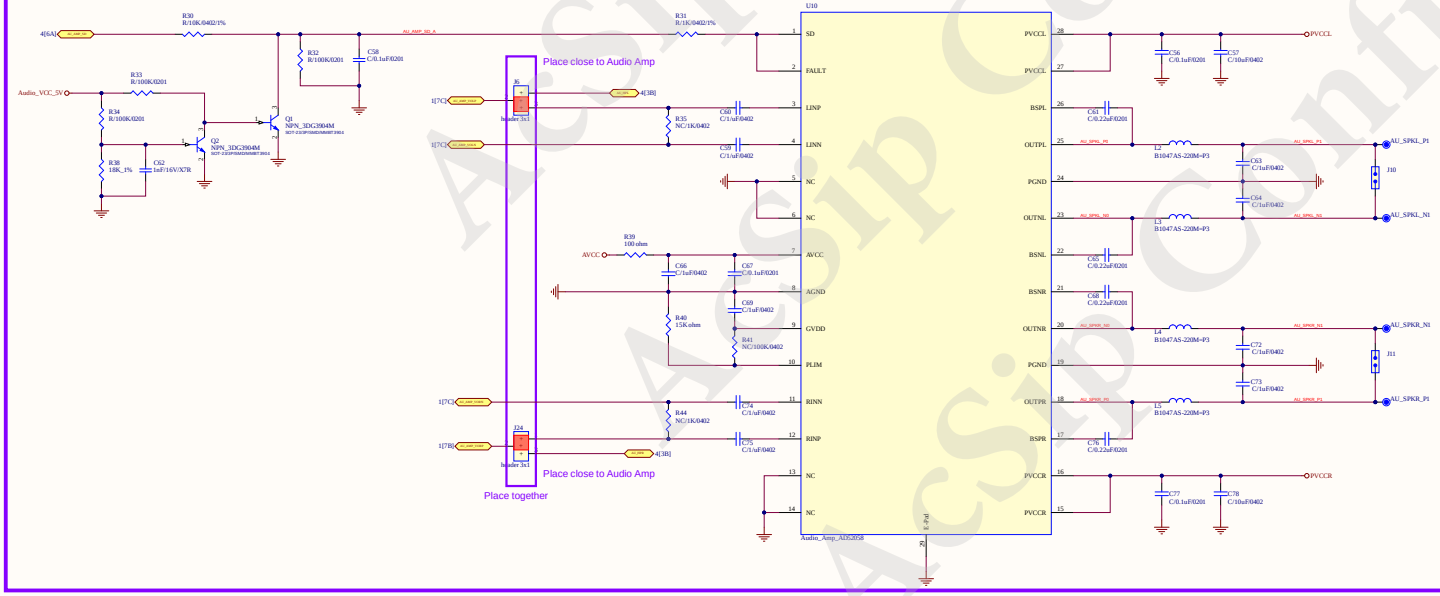
Line-Out



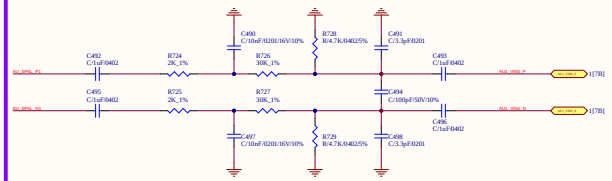
Microphone (Analog MIC)



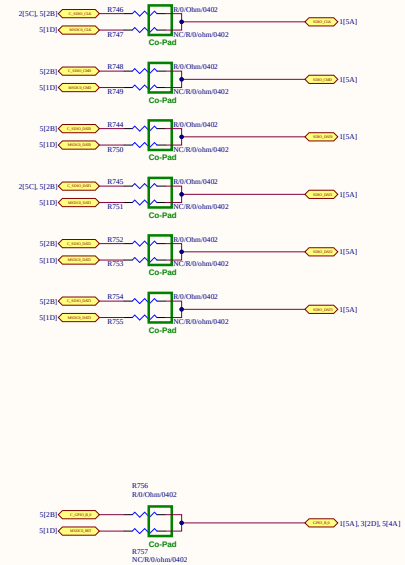
Audio Amp

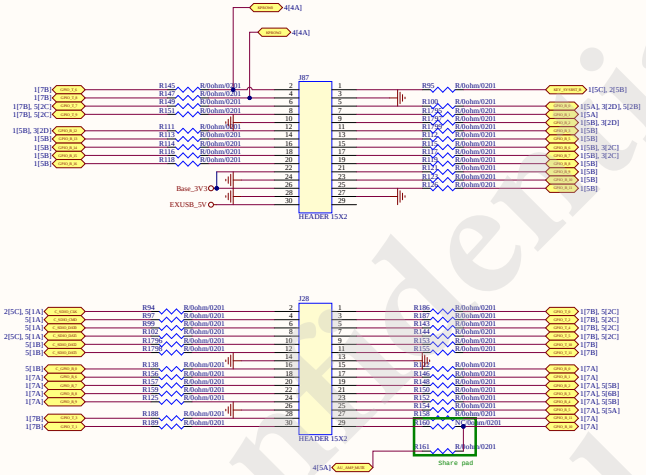


AEC External Loop Back Circuit

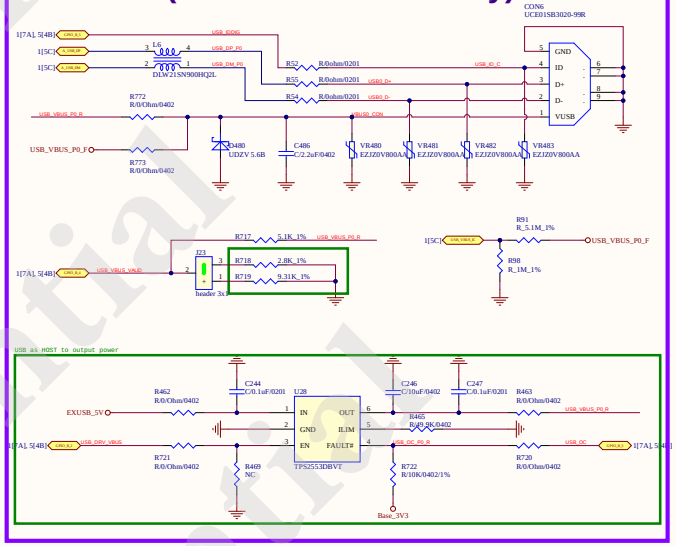


GPIO

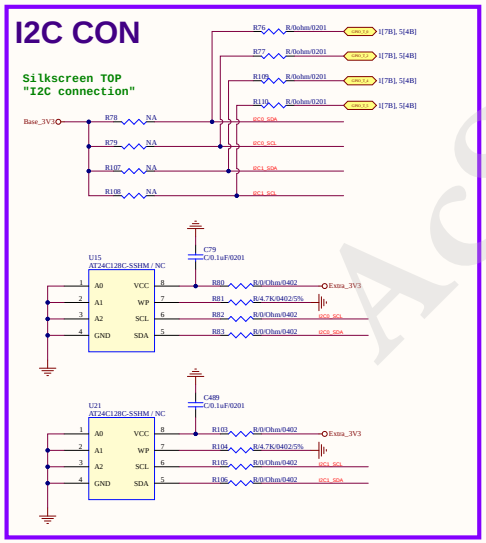




USB CON (AI7933CLD / ALD Only)

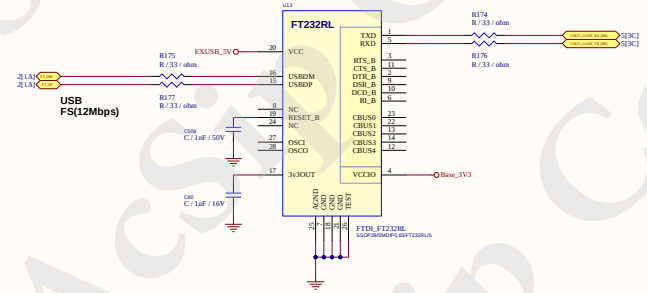


I2C CON

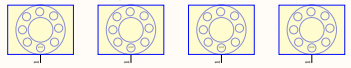


UART Connection

FTDI



HOLE



SD Card