APPLICATION NOTE

Product Name	**AI7688H** **MT7688 IoT SiP Module**
Version	**F**
Doc No	**902-09003**
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Document History

Date	Revised Contents	Revised By	Version
May 11th,2016	Initial release	Kevin	A
Jun 23th,2016	Modify SD Schematic	Kevin	B
Oct 27th,2016	SPI Master bus info. Added	Kevin	C
Oct 24th,2017	MDI_Pin Precautions for use	Ivan	D
Aug 07th,2018	I-PEX MHF4 connector Precautions for use	Ivan	E
Mar 15th,2019	Bootstrapping Pins Description and setup	Jack	F

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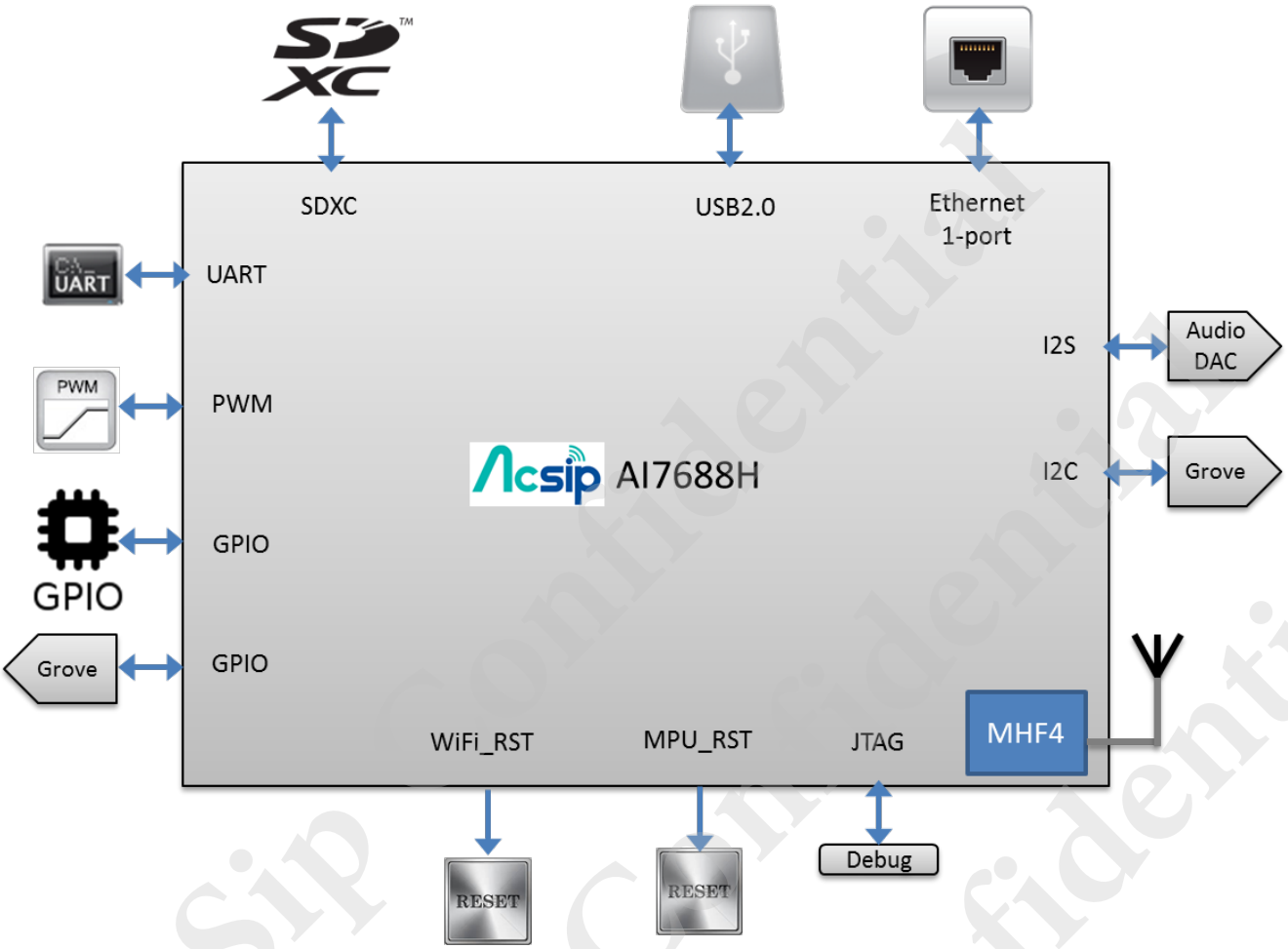
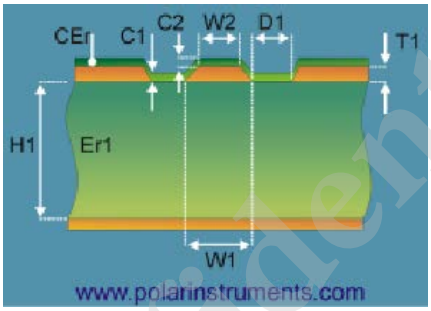
1. Typical application



2. Layout Guide

2-1. RF Layout (Pin_Out_60)

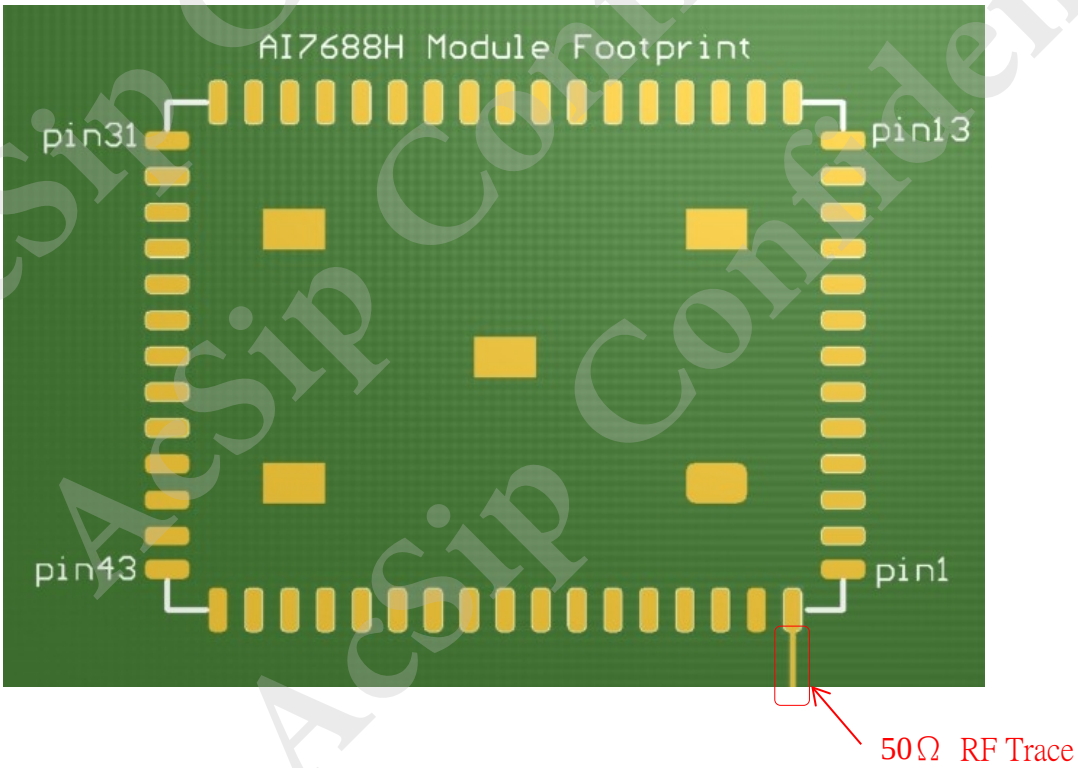
CPWG model is recommended for RF trace calculation, which has better EMC and RF capability. And please discuss with PCB manufacturer to evaluate and keep RF trace in 50ohm.



Note: Suggest reserving matching circuit between module and Antenna.

2-1-1 Pin_Out_60 (2.4G_RF) precautions for use

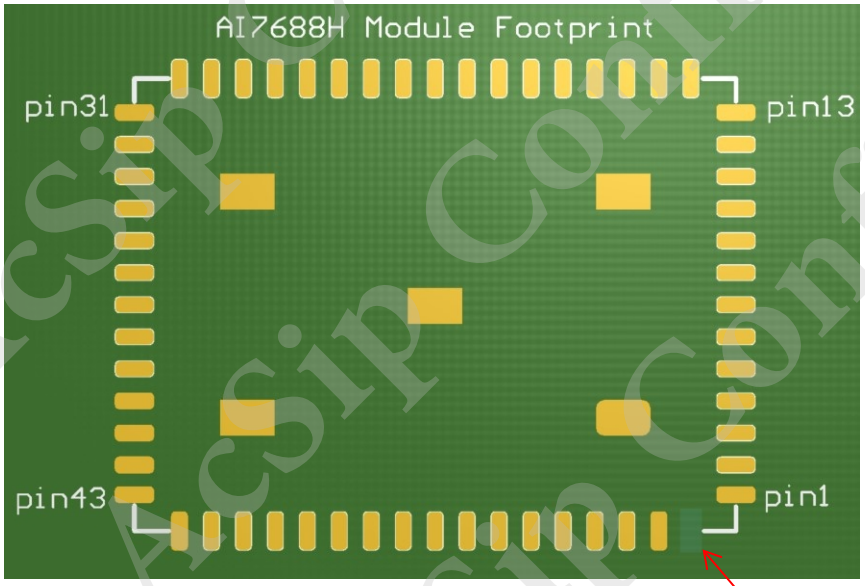
When using the pin_60 (2.4G_RF) as the RF output, the layout RF trace impedance must be 50Ω



2-1-2 I-PEX MHF4 Connector precautions for use

When using the I-PEX MHF4 connector for RF output, AI7688H module pin_60(2. 4G_RF) don't need to build PCB pad

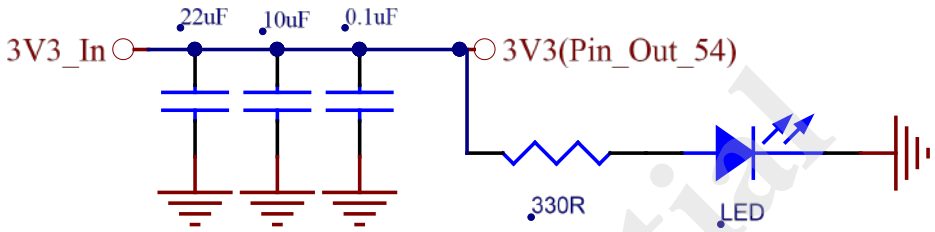
Using the I-PEX MHF4 connector for RF-output



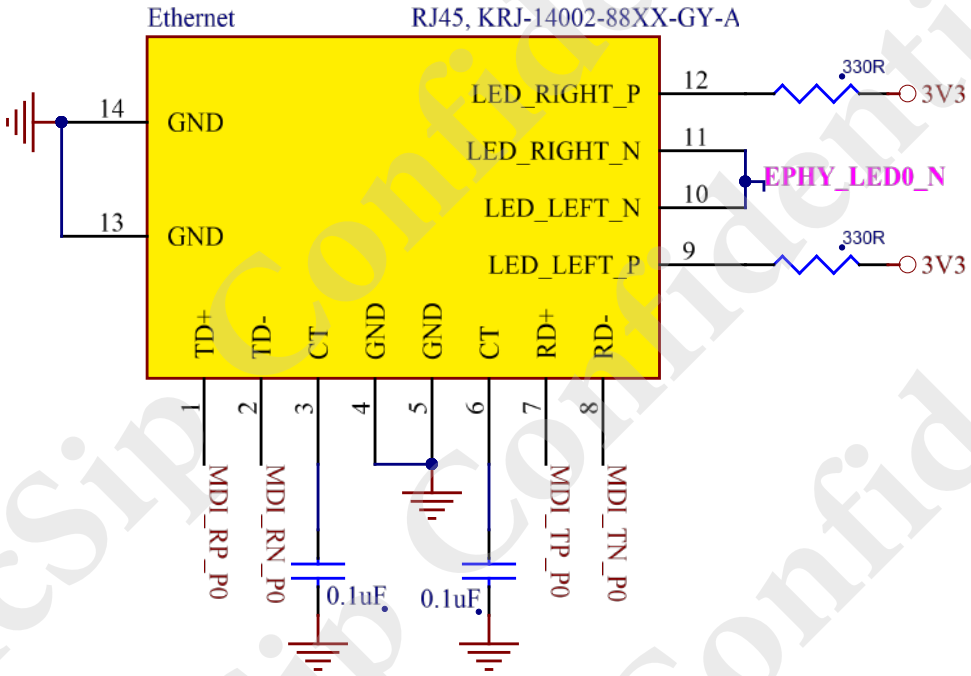
Pin_60 does not need to connect the PCB pad

2-2. DC Power

The 3V3 power trace width should be >=40mil



2-3. Ethernet Schematic



•Separate each Ethernet pairs with “well GND shielding”

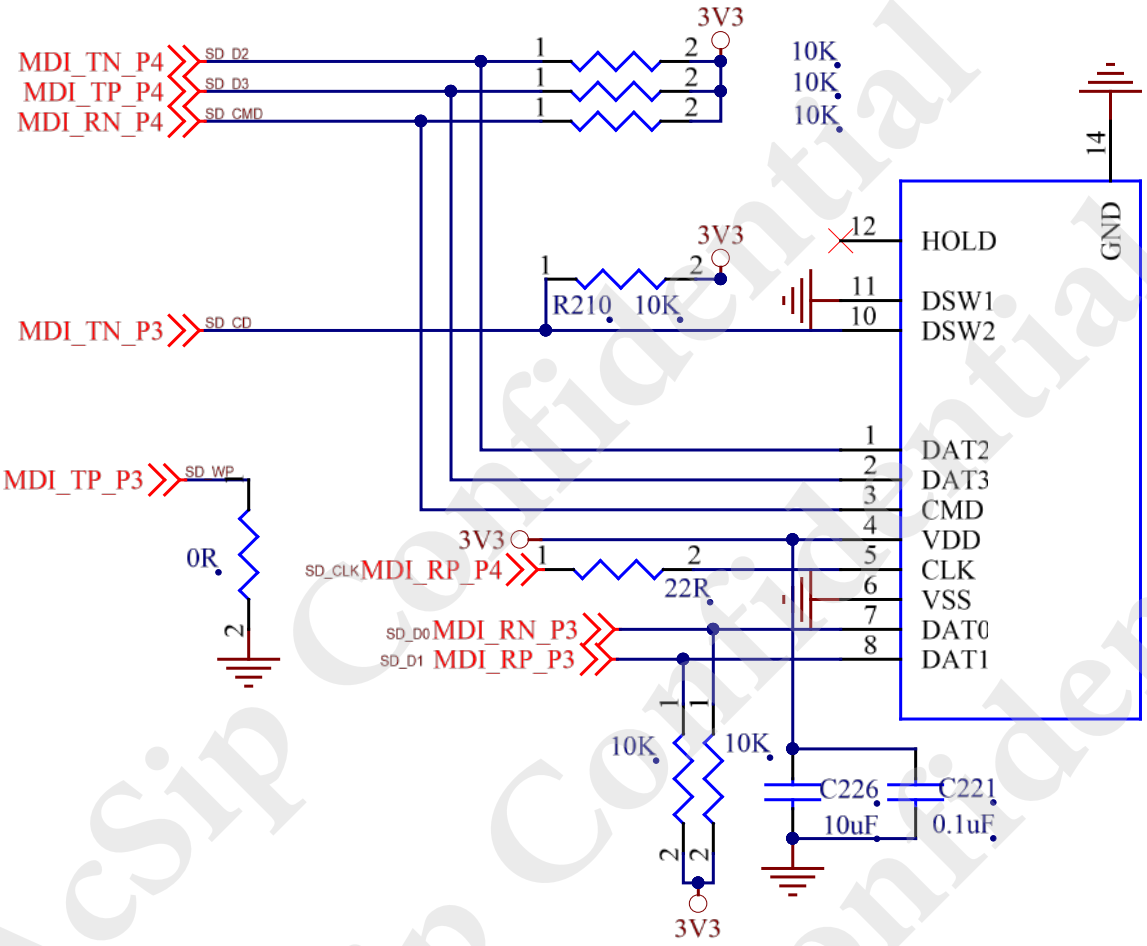
•Impedance is 100-ohm (differential)

•With >80mil gap between ethernet GND plane & system GND plane

•Ethernet pair between transformer & RJ-45 connector should meet width/space=18/5mil

2-4. SD Schematic

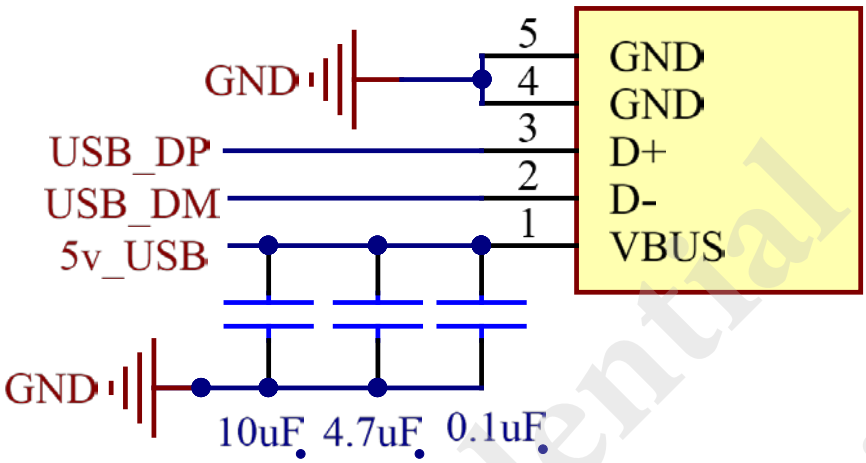
Please make sure the selected SD tray behavior is matching the table shown as below, in order to keep SD functionality.



SWITCH	WITHOUT CARD	WITH CARD
	DSW1 DSW2 ④ ⑤ ⑥ GND GND SD_CD Pull Low	DSW1 DSW2 ④ ⑤ ⑥ GND GND SD_CD Pull high

		CONTACT AREA	TERMINAL AREA
①	CONTACT	Au (0.5μm MIN) OVER Ni (2μm MIN)	Au FLASH (0.03μm MIN) OVER Ni (1μm MIN)
⑤	DETECTION SWITCH 1(DSW1)	Au (0.1μm MIN) OVER Ni (1μm MIN)	
⑥	DETECTION SWITCH 2(DSW2)		
④	TOP COVER	-	Au FLASH (0.03μm MIN)

2-5. USB Schematic

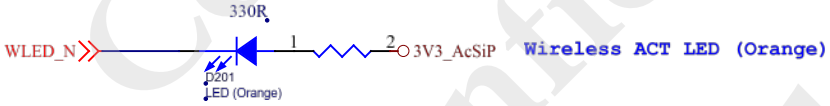


•Keep USB_DP / DM differential pairs routing with well “GND shielding”

•Impedance is 90-ohm (differential)

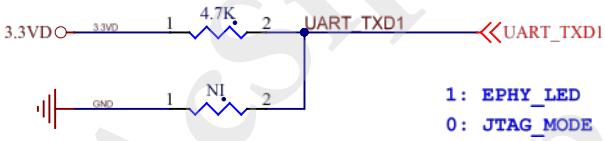
•USB_5V power trace >=20mil

2-6. LED Schematic



2-7. Other Schematic

•JTAG MODE

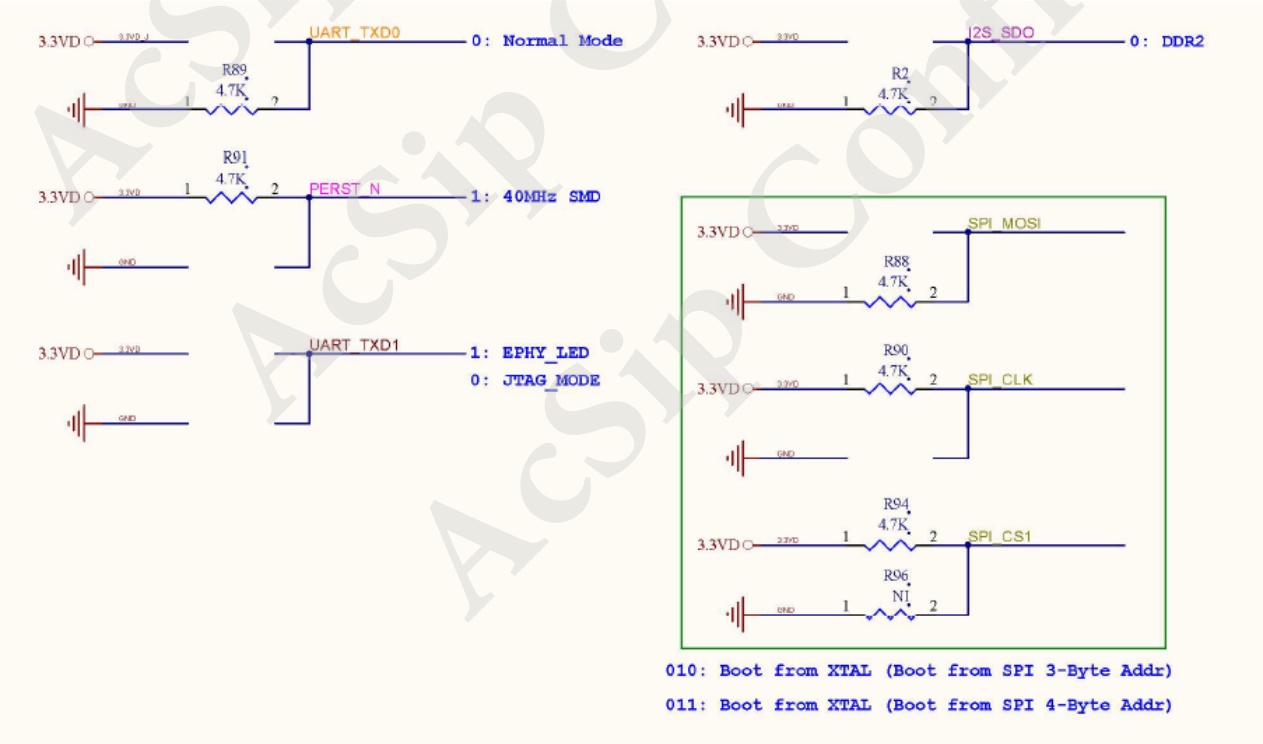


•MPU Reset / WIFI Reset

•Bootstrapping Pins Description and setup

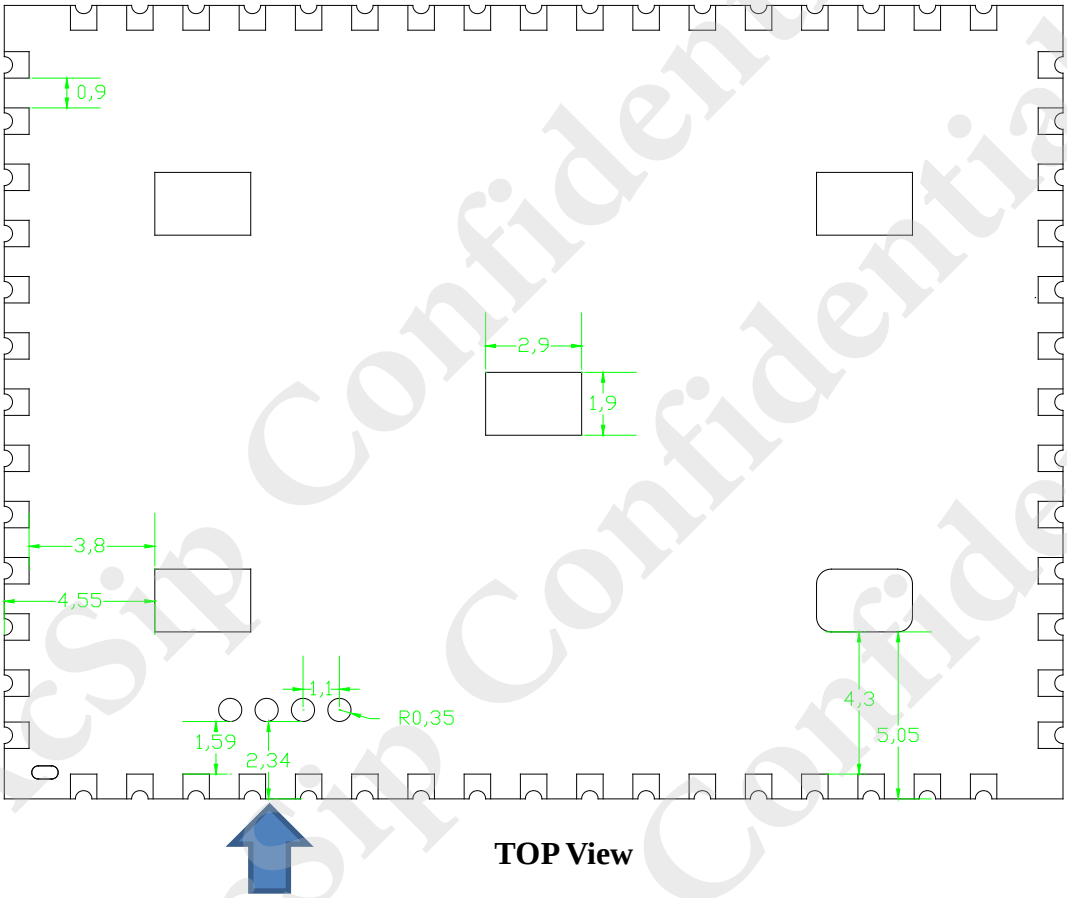
Pin Name	Boot Strapping Signal Name	Description	AI7688 internal setup
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)	
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD	1
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7688AN only. It needs to be pull-low for 7688KN which only supports DDR1.	0
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)	011
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)	0

Bootstrapping circuit of AI7688H internal setup.



2-8. SPI (Master) Schematic

AI7688H has 4 pins: SPI_MOSI, SPI_MISO, SPI_CLK, and SPI_CS1 for SPI master bus. It's important to notice that these pins are also connected to the module internal flash. Be mindful when you perform operation with them, or the flash may be inaccessible. Developers should access the SPI functionality through SPI modules only and avoid treating these SPI pins as general GPIO, otherwise, the flash storage may work incorrectly.

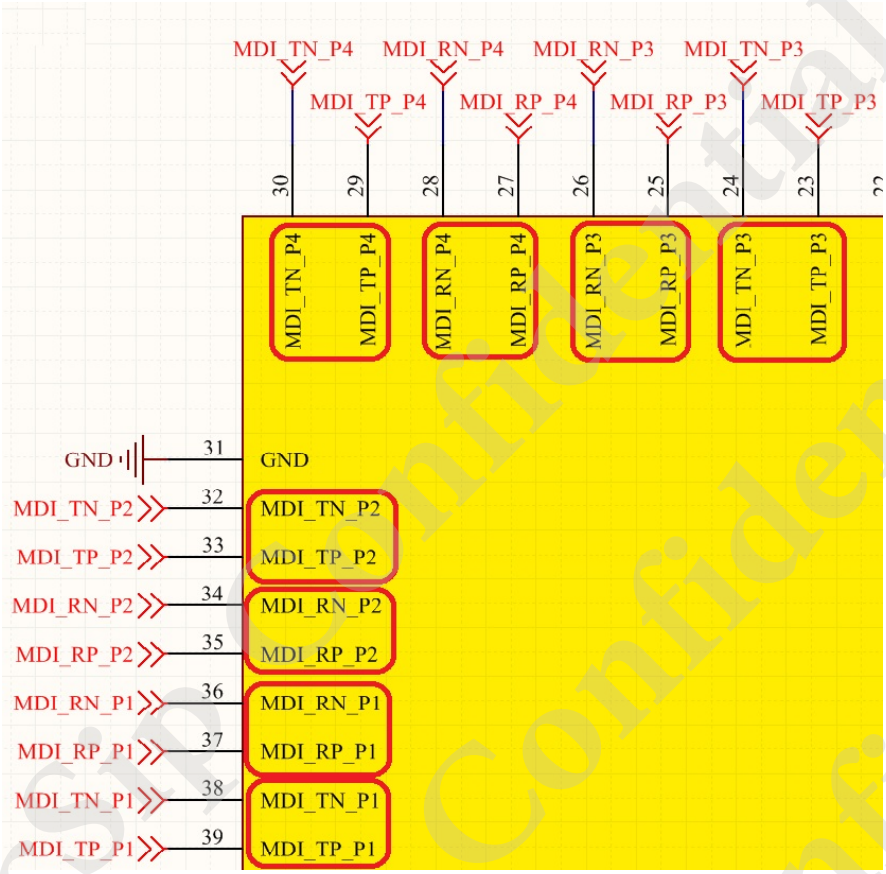


TOP View

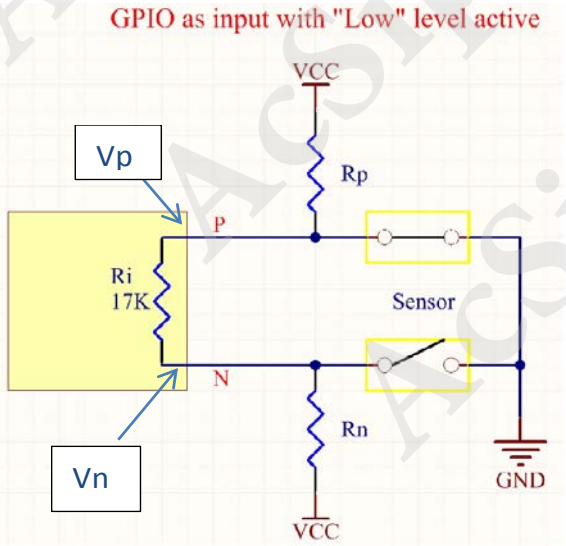
SPI Pin Out

2-9. MDI_Pin Precautions for use

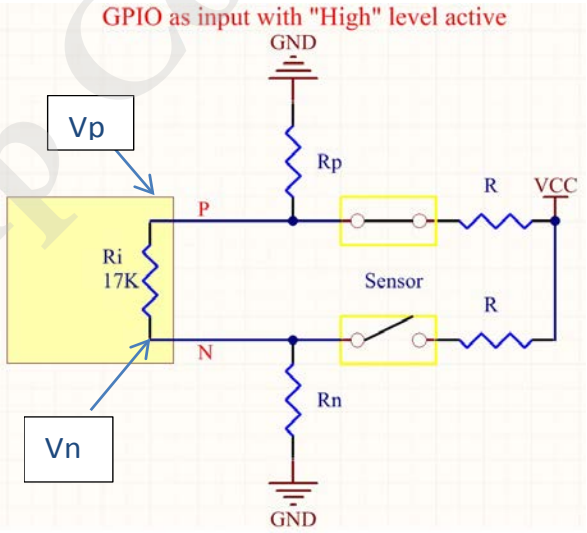
MT7688AN's differential pin (Figure 1) When using the GPIO function and set to the input pin, the same group of pins (P / N) will produce leakage current. Need to consider the design pull-up (Figure 2) or pull down (Figure 3) resistor (Rp / Rn).



(figure 1)



(figure 2)



(figure 3)

For example, if the differential pins are used for input and detect “low”. It has to pull-high as figure 2.
When sensor/device send “low” to differential “P” (Vp=0V), and differential “N” is open.
Then Vn will get voltage and it could result in the error level decision.

Vn= Vcc*(Ri/(Ri+Rn))

If Vcc=3.3V, Rn=4.7k then, Vn=3.3(17k/(17k+4.7k))=2.585V
If Vcc=3.3V, Rn=20k then, Vn=3.3(17k/(17k+20k))=1.5V
If Vcc=3.3V, Rn=100k then, Vn=3.3(17k/(17k+100k))=0.48V

You have to consider the resister value of Rp/Rn. Also the input level for P/N have to the same situation (Low active or High active for differential “P”, “N” input).Or only use differential “P”(“N”) and opening “N”(“P”.)

3. Other information

- Do not put any signal line or power line on system PCB top layer under AI7688H module.
- Discuss with AcSiP’s engineer after schematic and layout finished.