

# APPLICATION NOTE

<b>Product Name</b>	<b>ST50H</b>
<b>Version</b>	<b>I</b>
<b>Doc No</b>	<b>902-12601</b>
<b>Date</b>	<b>2022/11/08</b>



## Document History

Date	Revised Contents	Revised By	Version
2020/03/26	Initial Version	PW	A
2020/05/15	Update Pin Definition	PW	B
2020/06/17	Add Pi-circuit description & ESD protection	PW	C
2020/07/09	Add RF switch control table	PW	D
	Add contact information		
2020/11/17	Add Vbat function/GPIO Alternate functions/Additional functions	Jack	E
2021/01/26	Harmonic suppression	Jack	F
2021/07/14	Harmonic suppression	Jack	G
2021/10/13	ST-LINK SWD Port	Jack	H
	VDD/VDDRF/VDDPA bypass capacitors		
2022/11/08	Add clock source characteristics	Kenny	I



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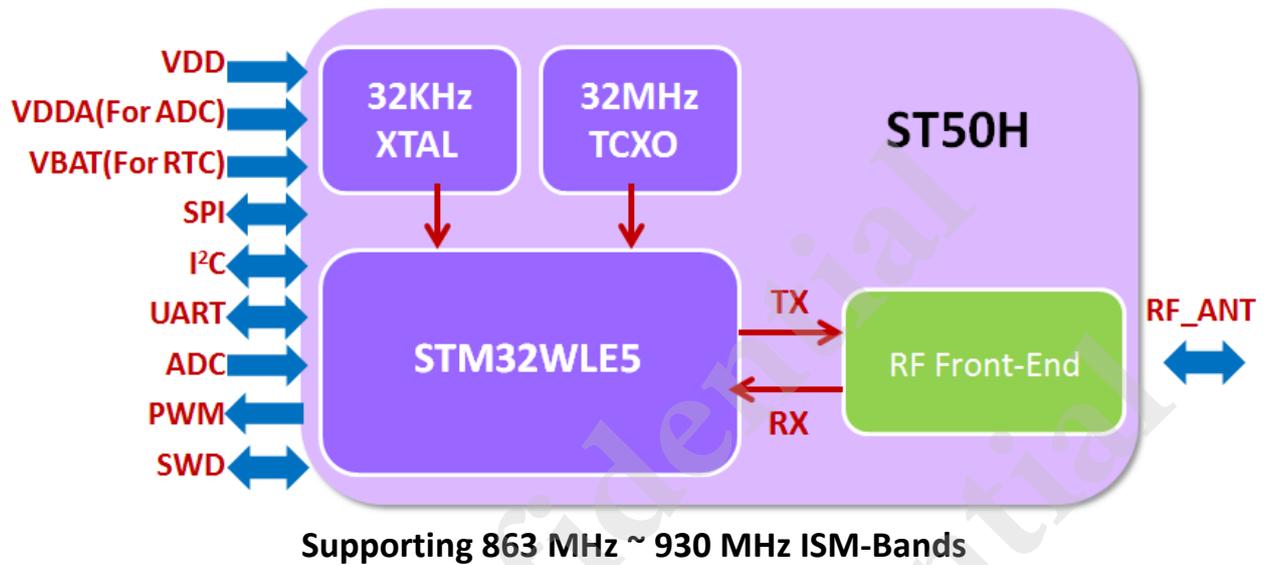
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## 1. Block Diagram

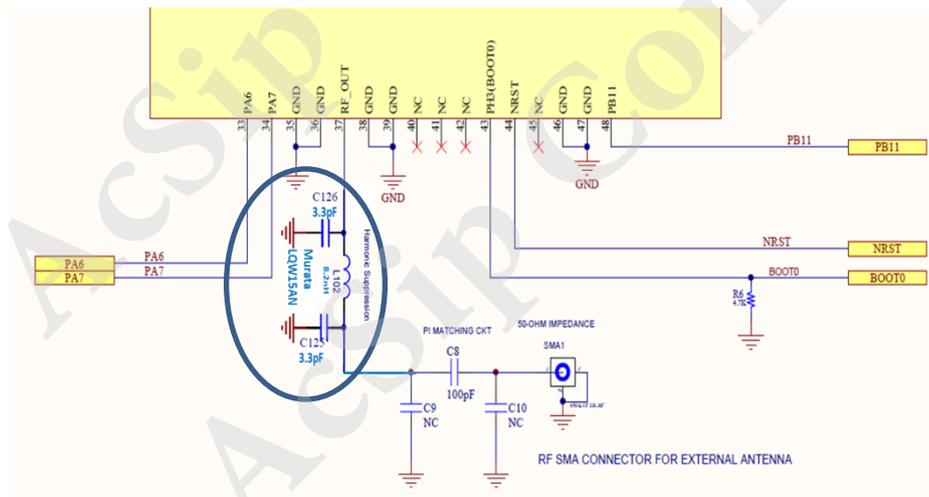


## 2. Application Circuit

### 2.1. Schematic

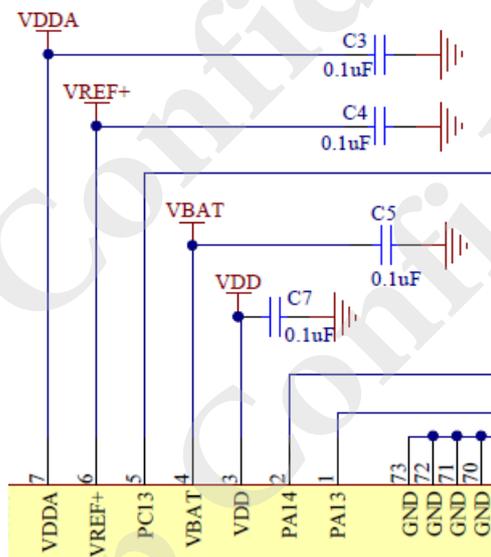
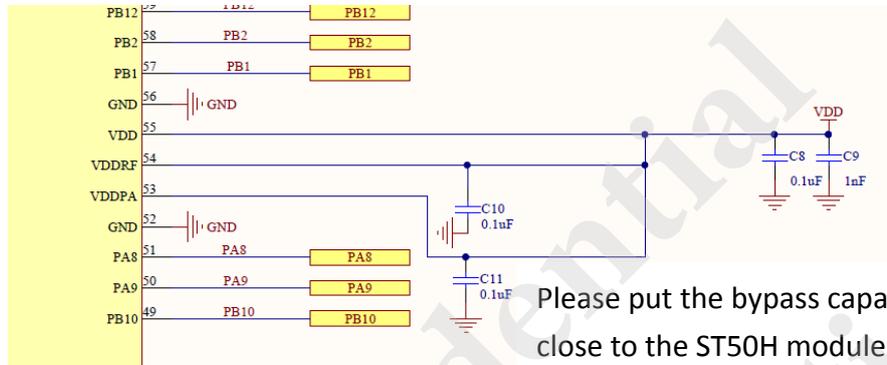
- RF

Please place harmonic suppression circuit close to module out.

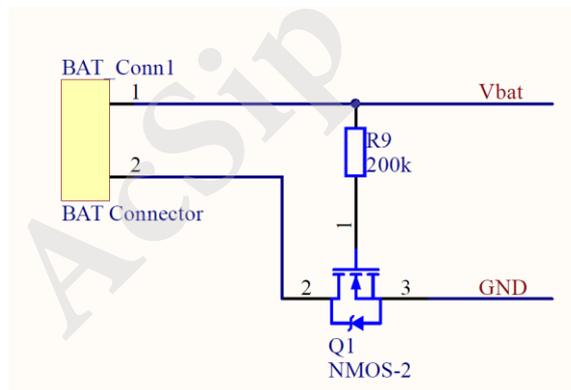


## ● Power

An independent LDO Buck or Boost for  $V_{in}$  regulating to  $V_{DD}(3.3V)$  is recommend for ST50H. Please place the LDO Buck or Boost as close as possible to ST50H.



## ● Battery protection



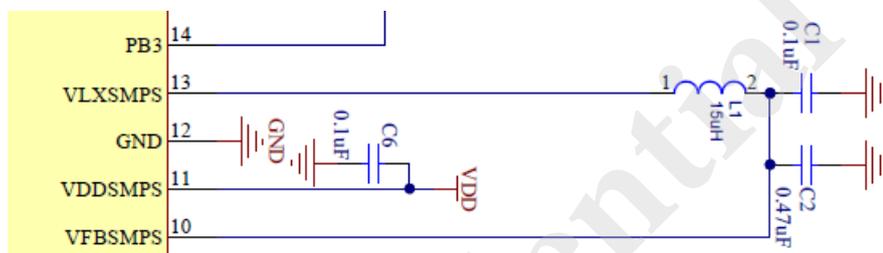
## ● Inductor

The L1 (15 $\mu$ H) consideration and recommended:

DCR (max) = 2 ohms

Idc (min) = 100 mA

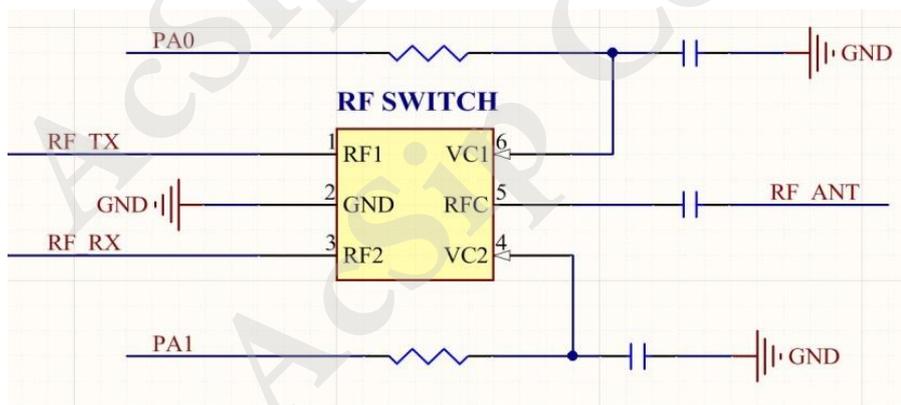
Freq (min) = 20 MHz



Reference	Manufacturer	Value ( $\mu$ H)	Idc max (mA)	Freq (MHz)	DCR (ohm)	Package (L x W x H in mm)
LPS3010-153	Coilcraft	15	370	43	0.95	2.95 x 2.95 x 0.9
MLZ2012N150L	TDK	15	90	40	0.47	2 x 1.25 x 1.25
MLZ2012M150W	TDK	15	120	40	0.95	2 x 1.25 x 1.25
VLS2010ET-150M	TDK	15	440	40	1.476	2 x 2 x 1
VLS2012ET-150M	TDK	15	440	40	1.062	2 x 2 x 1.2

## ● RF Switch Control Table

VC1(PA0)	VC2(PA1)	RF_TX-RF_ANT	RF_RX-RF_ANT
High	Low	Off	On
Low	High	On	Off



## 2.2. Power Supply Management

The devices embed two different regulators: one LDO and one DC/DC (SMPS). The SMPS can be optionally switched-on by software to improve the power efficiency. As LDO and SMPS operate in parallel, the SMPS switch-on is transparent to the user and only the power efficiency is affected.

### 2.2.1. Power Supply Schemes

The devices require a VDD operating voltage supply between 1.8 V and 3.6 V. Several independent supplies (VDDSMPS, VFBSMPS, VDDA, VDDRF) can be provided for specific peripherals:

- **VDD = 1.8 V to 3.6 V**  
VDD is the external power supply for the I/Os, the system analog blocks such as reset, power management, internal clocks and low-power regulator. It is provided externally through VDD pins.
- **VDDSMPS = 1.8 V to 3.6 V**  
VDDSMPS is the external power supply for the SMPS step-down converter. It is provided externally through VDDSMPS supply pin and must be connected to the same supply as VDD.
- **VFBSMPS = 1.45 V to 1.62 V (1.55 V typical)**  
VFBSMPS is the external power supply for the main system regulator. It is provided externally through VFBSMPS pin and is supplied through the SMPS step-down converter.
- **VDDA = 0 V to 3.6 V (DAC minimum voltage is 1.71 V without buffer and 1.8 V with buffer. COMP and ADC minimum voltage is 1.62 V. VREFBUF minimum voltage is 2.4 V)**  
VDDA is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, and comparators. The VDDA voltage level is independent from the VDD voltage (see power-up and power-down limitations below) and must preferably be connected to VDD when these peripherals are not used.
- **VDDRF = 1.8 V to 3.6 V**  
VDDRF is an external power supply for the radio. It is provided externally through the VDDRF pin and must be connected to the same supply as VDD.
- **VBAT = 1.55 V to 3.6 V**  
VBAT is the power supply for RTC, TAMP, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

- **VREF-, VREF+**

VREF+ is the input reference voltage for ADC and DAC. It is also the output of the internal voltage reference buffer when enabled.

- When  $VDDA < 2\text{ V}$ , VREF+ must be equal to VDDA.
- When  $VDDA \geq 2\text{ V}$ , VREF+ must be between 2 V and VDDA.

VREF+ can be grounded when ADC/DAC is not active. The internal voltage reference buffer supports the following output voltages, configured with VRS bit in the VREFBUF\_CSR register:

- VREF+ around 2.048 V: this requires  $VDDA \geq 2.4\text{ V}$ .
- VREF+ around 2.5 V: this requires  $VDDA \geq 2.8\text{ V}$ .

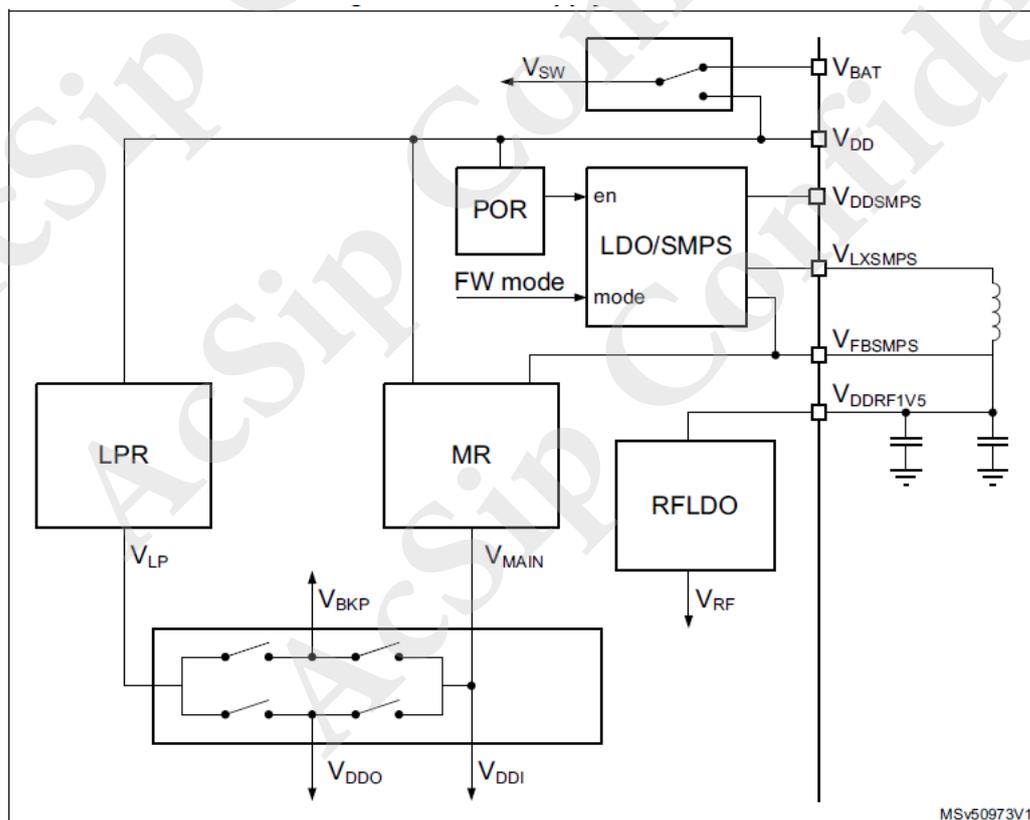
During power up and power down, the following power sequence is required:

1. When  $VDD < 1\text{ V}$  other power supplies (VDDA) must remain below  $VDD + 300\text{ mV}$ .

During power down, VDD can temporarily become lower than other supplies only if the energy provided to the device remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during this transient phase.

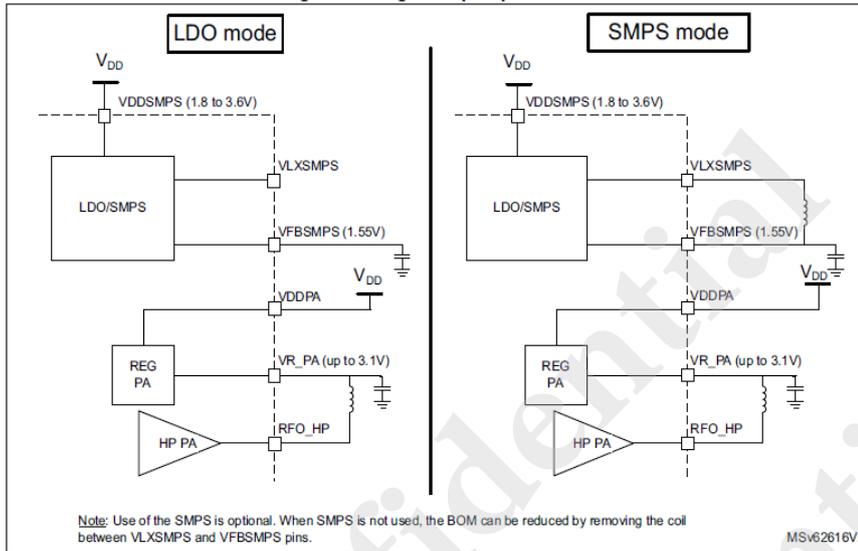
2. When  $VDD > 1\text{ V}$ , all other power supplies (VDDA) become independent.

An embedded linear voltage regulator is used to supply the internal digital power V<sub>CORE</sub>. V<sub>CORE</sub> is the power supply for digital peripherals, SRAM1 and SRAM2. The Flash memory is supplied by V<sub>CORE</sub> and VDD. V<sub>CORE</sub> is split in two parts: VDDO part and an interruptible part VDDI.



- VDDPA:**

Transmit high output power up to + 22 dBm, VDDPA must be supplied directly from VDD on VDDSMPS pin, as shown in the figure below.

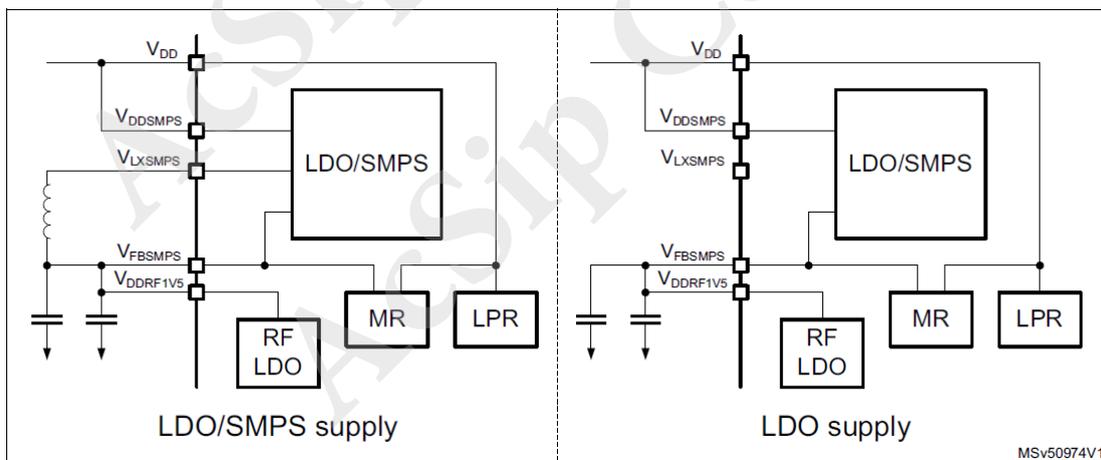


The output power range is programmable in 32 steps of ~ 1 dB. The power amplifier ramping timing is also programmable. This allows adaptation to meet radio regulation requirements. The table below gives the maximum transmit output power versus the VDDPA supply level.

VDDPA supply (V)	Transmit output power (dBm)
3.3	+ 22
2.7	+ 20
2.4	+ 19
1.8	+ 16

## 2.2.2. Power Supply configurations

The different supply configurations are shown in the figure below.



The LDO or SMPS step-down converter operating mode can be configured by one of the following:

- by the MCU using the SMPSEN setting in PWR control register 5 (PWR\_CR5), that depends upon the MCU system operating mode (Run, Stop, Standby or Shutdown).
- by the sub-GHz radio using SetRegulatorMode() command and the sub-GHz radio operating mode (Sleep, Calibrate, Standby, Standby with HSE32 or Active).

After any POR and NRST reset, the LDO mode is selected. The SMPS selection has priority over LDO selection.

While the sub-GHz radio is in Standby with HSE32 or in Active mode, the supply mode is not altered until the sub-GHz radio enters Standby or Sleep mode. The sub-GHz radio activity may add a delay for entering the MCU software requested supply mode.

The LDO or SMPS supply mode can be checked with the SMPSRDY flag in power status register 2 (PWR\_SR2).

Note: When the radio is active, the supply mode is not changed until after the radio activity is finished.

During Stop 1, Stop 2 and Standby modes, when the sub-GHz radio is not active, the LDO or SMPS step-down converter is switched off. When exiting low-power modes (except Shutdown), the SMPS step-down converter is set by hardware to the mode selected by the SMPSEN bit in PWR control register 5 (PWR\_CR5). SMPSEN is retained in Stop and Standby modes.

Independently from the MCU software selected supply operating mode, the sub-GHz radio allows the supply mode selection while the sub-GHz radio is active (thanks to the sub-GHz radio SetRegulatorMode() command).

The maximum load current delivered by the SMPS can be selected by the sub-GHz radio SUBGHZ\_SMPSC2R register.

The inrush current of the LDO and SMPS step-down converter can be controlled via the sub-GHz radio SUBGHZ\_PCR register. This information is retained in all but the sub-GHz radio Deep-sleep mode.

The SMPS needs a clock to be functional. If for any reason this clock stops, the device may be destroyed. To avoid this situation, a clock detection is used to, in case of a clock failure, switch off the SMPS and enable the LDO. The SMPS clock detection is enabled by the sub-GHz radio SUBGHZ\_SMPSCOR.CLKDE. By default, the SMPS clock detection is disabled and must be enabled before enabling the SMPS.

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**Danger:** Before enabling the SMPS, the SMPS clock detection must be enabled in the sub-GHz radio SUBGHZ\_SMPSCOR.CLKDE.

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## 2.2.3. Power supply supervisor

The devices integrate a power-on reset/power-down reset, coupled with a Brownout reset (BOR) circuitry.

BOR0 level cannot be disabled. Other BOR levels can be enabled by user option. When enabled, BOR is active in all power modes except in Shutdown. Five BOR thresholds can be selected through option bytes.

During power-on, BOR keeps the device under reset until the supply voltage VDD reaches the specified VBORx threshold:

- When VDD drops below the selected threshold, a device reset is generated.
- When VDD is above the VBORx upper limit, the device reset is released and the system can start.

The devices feature an embedded PVD (programmable voltage detector) that monitors the VDD power supply and compares it with the VPVD threshold. An interrupt can be generated when VDD drops below the VPVD threshold and/or when VDD is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state.

The PVD is enabled by software and can be configured to monitor the VDD supply level needed for the sub-GHz radio operation. For this, the PVD must select its lowest threshold, and the PVD and the wakeup must be enabled by the EWPVD bit in PWR\_CR3 register.

Only a voltage drop below the PVD level generates a wakeup event.

In addition, the devices embed a PVM (peripheral voltage monitor) that compares the independent supply voltage VDDA with a fixed threshold to ensure that the peripheral is in its functional supply range.

Finally, a radio end-of-life monitor provides information on the VDD supply when VDD is too low to operate the sub-GHz radio. When reaching the EOL level, the software must stop all radio activity in a safe way.

## 2.2.4. Linear voltage regulator

Two embedded linear voltage regulators supply all the digital circuitries, except for the Standby circuitry and the Backup domain. The main regulator (MR) output voltage (VCORE) can be programmed by software to two different power ranges (range 1 and range 2), to optimize the consumption depending on the system maximum operating frequency.

The voltage regulators are always enabled after a reset. Depending on the application modes, the VCORE supply is provided either by the main regulator or by the low-power regulator (LPR).

When MR is used, a dynamic voltage scaling is proposed to optimize power as follows:

- range 1: high-performance range

The system clock frequency can be up to 48 MHz. The Flash memory access time for read access is minimum. Write and erase operations are possible.

- range 2: low-power range

The system clock frequency can be up to 16 MHz. The Flash memory access time for a read access is increased as compared to range 1. Write and erase operations are possible.

## 2.2.5. VBAT

### The VBAT operation

The VBAT pin is used to power the device VBAT domain (RTC, LSE and backup registers) from an external battery, an external super-capacitor, or from VDD when no external battery nor an external super-capacitor are present. Three anti-tamper detection pins are available in VBAT mode. VBAT operation is automatically activated when VDD is not present.

An internal VBAT battery charging circuit is embedded and can be activated when VDD is present.

Note: When the microcontroller is supplied only from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

### VBAT battery voltage monitoring

This embedded hardware feature allows the application to measure the VBAT battery voltage using the ADC VIN[14] input channel. As VBAT may be higher than VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by three. As a consequence, the converted digital value is one third the VBAT voltage.

## 2.2.6. Low-power modes

The devices support several low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources. By default, the microcontroller is in Run mode, range 1, after a system or a power-on reset. It is up to the user to select one of the low-power modes described below:

- **Sleep mode:**

CPU clock off, all peripherals including CPU core peripherals (among them NVIC, SysTick) can run and wake up the CPU when an interrupt or an event occurs.

- **Low-power run mode (LPRun):**

when the system clock frequency is reduced below 2 MHz. The code is executed from the SRAM or from the Flash memory. The regulator is in low-power mode to minimize the operating current.

- **Low-power sleep mode (LPSleep):** entered from the LPRun mode.

- **Stop 0 and Stop 1 modes:**

the content of SRAM1, SRAM2 and of all registers is retained. All clocks in the VCORE domain are stopped. PLL, MSI, HSI16 and HSE32 are disabled. LSI and LSE can be kept running.

RTC can remain active (Stop mode with RTC, Stop mode without RTC). The sub-GHz radio may remain active independently from the CPU.

Some peripherals with the wakeup capability can enable HSI16 RC during the Stop mode to detect their wakeup condition.

- **Stop 1** offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption compared with Stop 2.

In Stop 0 mode, the main regulator remains on, resulting in the fastest wakeup time but with much higher consumption. The active peripherals and wakeup sources are the same as in Stop 1 mode that uses the low-power regulator.

The system clock, when exiting Stop 0 or Stop 1 mode, can be either MSI up to 48 MHz or HSI16, depending on the software configuration.

- **Stop 2** mode: part of the VCORE domain is powered off. Only SRAM1, SRAM2, CPU and some peripherals preserve their contents. All clocks in the VCORE domain are stopped. PLL, MSI, HSI16 and HSE32 are disabled.

LSI and LSE can be kept running.

RTC can remain active (Stop 2 mode with RTC, Stop 2 mode without RTC). The sub-GHz radio may also remain active independent from the CPU.

Some peripherals with the wakeup capability can enable HSI16 RC during the Stop 2 mode to detect their wakeup condition.

The system clock when exiting from Stop 2 mode, can be either MSI up to 48 MHz or HSI16, depending on the software configuration.

- **Standby mode:**

VCORE domain is powered off. However, it is possible to preserve the SRAM2 content as detailed below:

Standby mode with SRAM2 retention when the RRS bit is set in the PWR control register 3



(PWR\_CR3). In this case, SRAM2 is supplied by the low-power regulator.

Standby mode when the RRS bit is cleared in the PWR control register 3 (PWR\_CR3). In this case the main regulator and the low-power regulator are powered off.

All clocks in the VCORE domain are stopped. PLL, MSI, HSI16 and HSE32 are disabled.

LSI and LSE can be kept running.

The RTC can remain active (Standby mode with RTC, Standby mode without RTC). The sub-GHz radio and the PVD may also remain active when enabled independent from the CPU. In Standby mode, the PVD selects its lowest level.

The system clock, when exiting Standby modes, is MSI at 4 MHz.

- **Shutdown mode:**

VCORE domain is powered off. All clocks in the VCORE domain are stopped. PLL, MSI, HSI16, LSI and HSE32 are disabled. LSE can be kept running. The system clock when exiting the Shutdown mode, is MSI at 4 MHz. In this mode, the supply voltage monitoring is disabled and the product behavior is not guaranteed in case of a power voltage drop.

## 2.3. Pin Definition

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	O	Output only pin
Notes	Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset	

Pin Name (function after reset)	Pin Type	Alternate functions	Additional functions
PA2	I/O	LSCO, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT, DEBUG_PWR_LDORDY, CM4_EVENTOUT	LSCO
PA3	I/O	TIM2_CH4, I2S2_MCK, USART2_RX, LPUART1_RX, CM4_EVENTOUT	

<b>PA4</b>	I/O	RTC_OUT2, LPTIM1_OUT, SPI1_NSS, USART2_CK, DEBUG_SUBGHZSPI_NSSOUT, LPTIM2_OUT, CM4_EVENTOUT	
<b>PA5</b>	I/O	TIM2_CH1, TIM2_ETR, SPI2_MISO, SPI1_SCK, DEBUG_SUBGHZSPI_SCKOUT, LPTIM2_ETR, CM4_EVENTOUT	
<b>PA6</b>	I/O	TIM1_BKIN, I2C2_SMBA, SPI1_MISO, LPUART1_CTS, DEBUG_SUBGHZSPI_MISOOUT, TIM16_CH1, CM4_EVENTOUT	
<b>PA7</b>	I/O	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, COMP2_OUT, DEBUG_SUBGHZSPI_MOSIOUT, TIM17_CH1, CM4_EVENTOUT	
<b>PA8</b>	I/O	MCO, TIM1_CH1, SPI2_SCK/I2S2_CK, USART1_CK, LPTIM2_OUT, CM4_EVENTOUT	
<b>PA9</b>	I/O	TIM1_CH2, SPI2_NSS/I2S2_WS, I2C1_SCL, SPI2_SCK/I2S2_CK, USART1_TX, CM4_EVENTOUT	
<b>PA10</b>	I/O	RTC_REFIN, TIM1_CH3, I2C1_SDA, SPI2_MOSI/I2S2_SD, USART1_RX, DEBUG_RF_HSE32RDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INM, COMP2_INM, DAC1_OUT, ADC1_IN6
<b>PA11</b>	I/O	TIM1_CH4, TIM1_BKIN2, LPTIM3_ETR, I2C2_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_NRESET, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN7
<b>PA12</b>	I/O	TIM1_ETR, LPTIM3_IN1, I2C2_SCL, SPI1_MOSI, RF_BUSY, USART1_RTS, CM4_EVENTOUT	ADC1_IN8
<b>PA13</b>	I/O	JTMS-SWDIO, I2C2_SMBA, IR_OUT, CM4_EVENTOUT	ADC1_IN9
<b>PA14</b>	I/O	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT	ADC1_IN10
<b>PA15</b>	I/O	JTDI, TIM2_CH1, TIM2_ETR, I2C2_SDA, SPI1_NSS, CM4_EVENTOUT	COMP1_INM, COMP2_INP, ADC1_IN11
<b>PB1</b>	I/O	LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT	COMP2_INP, ADC1_IN5

<b>PB2</b>	I/O	LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, DEBUG_RF_SMPSTRDY, CM4_EVENTOUT	COMP1_INP, COMP2_INM, ADC1_IN4
<b>PB3</b>	I/O	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, RF_IRQ0, USART1_RTS, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC1_IN2, TAMP_IN3/ WKUP3
<b>PB4</b>	I/O	NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_LDORDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INP, COMP2_INP, ADC1_IN3
<b>PB5</b>	I/O	LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, RF_IRQ1, USART1_CK, COMP2_OUT, TIM16_BKIN, CM4_EVENTOUT	
<b>PB6</b>	I/O	LPTIM1_ETR, I2C1_SCL, USART1_TX, TIM16_CH1N, CM4_EVENTOUT	
<b>PB7</b>	I/O	LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT	
<b>PB8</b>	I/O	TIM1_CH2N, I2C1_SCL, RF_IRQ2, TIM16_CH1, CM4_EVENTOUT	
<b>PB9</b>	I/O	TIM1_CH3N, I2C1_SDA, SPI2_NSS/I2S2_WS, IR_OUT, TIM17_CH1, CM4_EVENTOUT	
<b>PB10</b>	I/O	TIM2_CH3, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_RX, COMP1_OUT, CM4_EVENTOUT	
<b>PB11</b>	I/O	TIM2_CH4, I2C3_SDA, LPUART1_TX, COMP2_OUT, CM4_EVENTOUT	
<b>PB12</b>	I/O	TIM1_BKIN, I2C3_SMBA, SPI2_NSS/I2S2_WS, LPUART1_RTS, CM4_EVENTOUT	
<b>PB13</b>	I/O	TIM1_CH1N, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_CTS, CM4_EVENTOUT	ADC1_IN0
<b>PB14</b>	I/O	TIM1_CH2N, I2S2_MCK, I2C3_SDA, SPI2_MISO, CM4_EVENTOUT	ADC1_IN1
<b>PB15</b>	I/O	TIM1_CH3N, I2C2_SCL, SPI2_MOSI/I2S2_SD, CM4_EVENTOUT	

<b>PC0</b>	I/O	LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, CM4_EVENTOUT	
<b>PC1</b>	I/O	LPTIM1_OUT, SPI2_MOSI/I2S2_SD, I2C3_SDA, LPUART1_TX, CM4_EVENTOUT	
<b>PC2</b>	I/O	LPTIM1_IN2, SPI2_MISO, CM4_EVENTOUT	
<b>PC3</b>	I/O	LPTIM1_ETR, SPI2_MOSI/I2S2_SD, LPTIM2_ETR, CM4_EVENTOUT	
<b>PC4</b>	I/O	CM4_EVENTOUT	
<b>PC5</b>	I/O	CM4_EVENTOUT	
<b>PC6</b>	I/O	I2S2_MCK, CM4_EVENTOUT	
<b>PC13</b>	I/O	RTC_OUT1/RTC_TS, CM4_EVENTOUT	TAMP_IN1/RTC_OUT1/RTC_TS/WKUP2
<b>NRST</b>	I/O		
<b>PH3</b>	I/O	CM4_EVENTOUT	BOOT0
<b>VDD</b>	S		
<b>VDDPA</b>	S		
<b>VDDRF</b>	S		
<b>VBAT</b>	S		
<b>VREF+</b>	S		
<b>VDDA</b>	S		
<b>VFBSMPS</b>	S		
<b>VDDSMPS</b>	S		
<b>VLXSMPS</b>	S		
<b>RF_OUT</b>	I/O		

Pin	Definition	ST50H Alternate functions															Additional functions		
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14		AF15	-
		SYS_AF	TIM1/TIM2/LPTIM1	TIM1/TIM2	SPI2S2TIM1/LPTIM3	I2C1/I2C2/I2C3	SPI1/SPI2S2	-	USART1/USART2	LPUART1	-	-	-	COMP1/COMP2/TIM1	DEBUG	TIM2/TIM16/TIM17/LPTIM2		EVENOUT	-
29	PA2	LSCO	TIM2_CH3	-	-	-	-	-	USART2_TX	LPUART1_TX	-	-	-	COMP2_OUT	DEBUG_PWR_LDORDY	-	CM4_EVENTOUT	LSCO	
30	PA3	-	TIM2_CH4	-	-	-	I2S2_MCK	-	USART2_RX	LPUART1_RX	-	-	-	-	-	-	CM4_EVENTOUT	-	
31	PA4	RTC_OUT2	LPTIM1_OUT	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	DEBUG_SUBGH_ZSPI_NSSOUT	LPTIM2_OUT	CM4_EVENTOUT	-	-	
32	PA5	-	TIM2_CH1	TIM2_ETR	SPI2_MISO	-	SPI1_SCK	-	-	-	-	-	-	DEBUG_SUBGH_ZSPI_SCKOUT	LPTIM2_ETR	CM4_EVENTOUT	-	-	
33	PA6	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI1_MISO	-	-	LPUART1_CTS	-	-	-	TIM1_BKIN	DEBUG_SUBGH_ZSPI_MISOOUT	TIM16_CH1	CM4_EVENTOUT	-	
34	PA7	-	TIM1_CH1N	-	-	I2C3_SCL	SPI1_MOSI	-	-	-	-	-	COMP2_OUT	DEBUG_SUBGH_ZSPI_MOSIOUT	TIM17_CH1	CM4_EVENTOUT	-	-	
51	PA8	MCO	TIM1_CH1	-	-	-	SPI2_SCK/I2S2_CK	-	USART1_CK	-	-	-	-	-	LPTIM2_OUT	CM4_EVENTOUT	-	-	
50	PA9	-	TIM1_CH2	-	SPI2_NSS/I2S2_WS	I2C1_SCL	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	-	-	-	-	CM4_EVENTOUT	-	-	
62	PA10	RTC_REFIN	TIM1_CH3	-	-	I2C1_SDA	SPI2_MOSI/I2S2_SD	-	USART1_RX	-	-	-	-	DEBUG_RF_HSE32RDY	TIM17_BKIN	CM4_EVENTOUT	COMP1_INM,COMP2_INM,DAC1_OUT,ADC1_IN6		
63	PA11	-	TIM1_CH4	TIM1_BKIN2	LPTIM3_ETR	I2C2_SDA	SPI1_MISO	-	USART1_CTS	-	-	-	-	TIM1_BKIN2	DEBUG_RF_NRESET	-	CM4_EVENTOUT	COMP1_INM,COMP2_INM,ADC1_IN7	
64	PA12	-	TIM1_ETR	-	LPTIM3_IN1	I2C2_SCL	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	-	CM4_EVENTOUT	ADC1_IN8		
1	PA13	JTMSJ/SWDIO	-	-	-	I2C2_SMBA	-	-	-	IR_OUT	-	-	-	-	-	CM4_EVENTOUT	ADC1_IN9		
2	PA14	JTCKJ/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	ADC1_IN10		
8	PA15	JTDI	TIM2_CH1	TIM2_ETR	-	I2C2_SDA	SPI1_NSS	-	-	-	-	-	-	-	-	CM4_EVENTOUT	COMP1_INM,COMP2_INP,ADC1_IN11		
57	PB1	-	-	-	-	-	-	-	-	LPUART1_RTS_DE	-	-	-	-	LPTIM2_IN1	CM4_EVENTOUT	COMP2_INP,ADC1_IN5		

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58	PB2	-	LPTIM1_OUT	-	-	I2C3_SMBA	SPI1_NSS	-	-	-	-	-	-	DEBUG_RF_SMPSTRDY	-	CM4_EVENTOUT	COMP1_INP,COMP2_INM,ADC1_IN4
14	PB3	JTDOJ TRACE SWO	TIM2_CH2	-	-	-	SPI1_SCK	-	USART1_RTS	-	-	-	-	-	-	CM4_EVENTOUT	COMP1_INM,COMP2_INM,ADC1_IN2,TAMP_IN3/WKUP3
15	PB4	NJTRST	-	-	-	I2C3_SDA	SPI1_MISO	-	USART1_CTS	-	-	-	-	DEBUG_RF_LDORDY	TIM17_BKIN	CM4_EVENTOUT	COMP1_INP,COMP2_INP,ADC1_IN3
16	PB5	-	LPTIM1_IN1	-	-	I2C1_SMBA	SPI1_MOSI	-	USART1_CK	-	-	-	COMP2_OUT	-	TIM16_BKIN	CM4_EVENTOUT	-
17	PB6	-	LPTIM1_ETR	-	-	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	TIM16_CH1N	CM4_EVENTOUT	-
18	PB7	-	LPTIM1_IN2	-	TIM1_BKIN	I2C1_SDA	-	-	USART1_RX	-	-	-	-	-	TIM17_CH1N	CM4_EVENTOUT	-
19	PB8	-	TIM1_CH2N	-	-	I2C1_SCL	-	-	-	-	-	-	-	-	TIM16_CH1	CM4_EVENTOUT	-
20	PB9	-	TIM1_CH3N	-	-	I2C1_SDA	SPI2_NSS/I2S2_WS	-	-	IR_OUT	-	-	-	-	TIM17_CH1	CM4_EVENTOUT	-
49	PB10	-	TIM2_CH3	-	-	I2C3_SCL	SPI2_SCK/I2S2_CK	-	-	LPUART1_RX	-	-	COMP1_OUT	-	-	CM4_EVENTOUT	-
48	PB11	-	TIM2_CH4	-	-	I2C3_SDA	-	-	-	LPUART1_TX	-	-	COMP2_OUT	-	-	CM4_EVENTOUT	-
59	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C3_SMBA	SPI2_NSS/I2S2_WS	-	-	LPUART1_RTS	-	-	-	-	-	CM4_EVENTOUT	-
60	PB13	-	TIM1_CH1N	-	-	I2C3_SCL	SPI2_SCK/I2S2_CK	-	-	LPUART1_CTS	-	-	-	-	-	CM4_EVENTOUT	ADC1_IN0
61	PB14	-	TIM1_CH2N	-	I2S2_MCK	I2C3_SDA	SPI2_MISO	-	-	-	-	-	-	-	-	CM4_EVENTOUT	ADC1_IN1
9	PB15	-	TIM1_CH3N	-	-	I2C2_SCL	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	-	CM4_EVENTOUT	-
21	PC0	-	LPTIM1_IN1	-	-	I2C3_SCL	-	-	-	LPUART1_RX	-	-	-	-	LPTIM2_IN1	CM4_EVENTOUT	-
22	PC1	-	LPTIM1_OUT	-	SPI2_MOSI/I2S2_SD	I2C3_SDA	-	-	-	LPUART1_TX	-	-	-	-	-	CM4_EVENTOUT	-
23	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-	-	-	-	-	-	-	CM4_EVENTOUT	-
24	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	LPTIM2_ETR	CM4_EVENTOUT	-
25	PC4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	-

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26	PC5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	-
27	PC6	-	-	-	-	-	I2S2_MCK	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	-
5	PC13	RTC_OUT1/ RTC_TS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	TAMP_IN1/RTC_OUT1/RTC_TS/WKUP2
43	PH3(BOOT0)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CM4_EVENTOUT	BOOT0
44	NRST	NRST																
3,55	VDD	VDD																
4	VBAT	VBAT																
53	VDDPA	VDDPA																
54	VDDRF	VDDRF																
6	VREF+	VREF+																
7	VDDA	VDDA																
10	VFBSMPS	VFBSMPS																
11	VDDSMPS	VDDSMPS																
13	VLXSMPS	VLXSMPS																
37	RF_OUT	RF_OUT																
12,28,35,36,38,39, 46,47,52,56 65~73		GND																
40,41,42,45		NC																

## 2.4. Clock source characteristics for ST50H

Clock source	Frequency	Accuracy	Trimming	
			Factory	User
HSE (TCXO)	32 MHz	TCXO dependent, down to few ppm	NA	Yes (optional)
LSE	32.768 kHz (typical)	Crystal dependent, down to a few ppm	NA	
HSI	16 MHz	± 0.8 % typical over -10 to +85 °C +0.1/-0.2 % typical over 1.8 V to 3.6 V	Yes	Yes
MSI	100 kHz 200 kHz 400 kHz 800 kHz 1 MHz 2 MHz 4 MHz 8 MHz 16 MHz 24 MHz 32 MHz 48 MHz	Default mode: +1.5/-1 % typical over -10 to +85 °C +1.5/-5.5 % typical for 16 to 48 MHz over 1.62 to 3.6 V PLL-mode: less than 0.25 %	Yes	Yes
LSI	32 kHz	±1.5 % typical over -40 to +125 °C +0.5/-1.5 % typical over 1.8 V to 3.6 V	Yes	No

In the application of industrial specification (-40~85°C) and high transmission rate, SYSCLK Source is recommended to use HSE.

## 3. Layout Guide

### 3.1. Power Trace Management

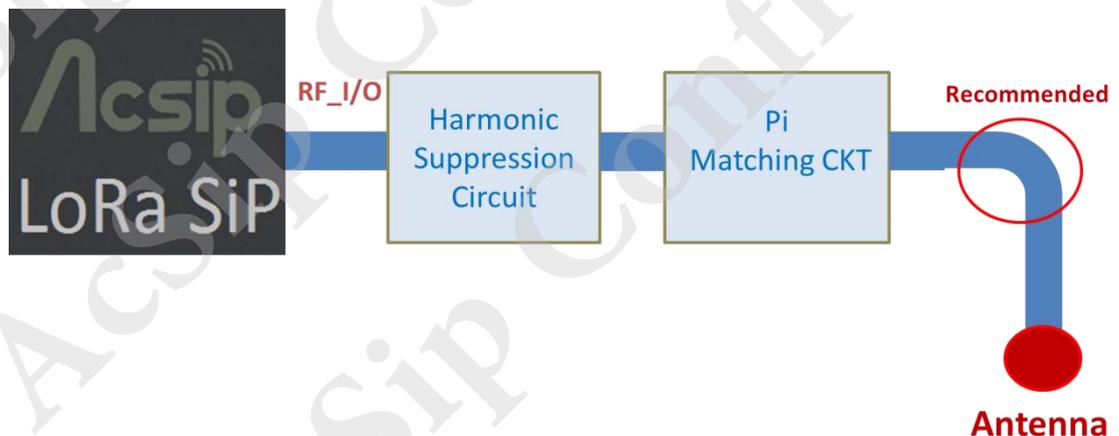
- Power traces should be directly connected with regulator outputs. And add 0.1uF bypass capacitors close to module on each power trace.
- Never let power trace cross the other one or high speed signal trace.

### 3.2. Ground Management

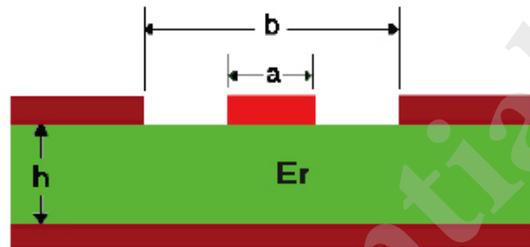
- Please ensure: (1). GND polygon regions used for module are as complete as possible and (2). well established GND via holes, to keep good heat dissipation and RF performance.
- The ref. ground planes of RF trace need to add via holes and we recommend the distance between each adding ones less than  $1/8\lambda$ .

### 3.3. RF Trace Management

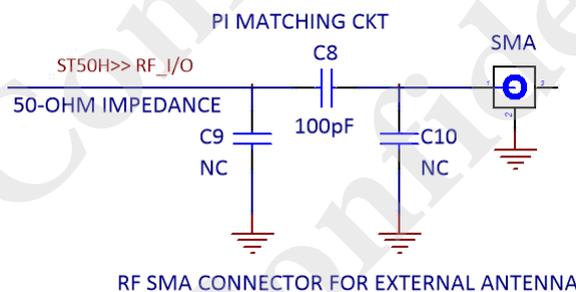
- CPWG model is recommended for RF trace calculation, which has better EMC and RF capability. And please discuss with PCB manufacturer to evaluate and keep RF trace in 50ohm.
- The recommended layout of RF trace bend is to keep the same width in the corner.



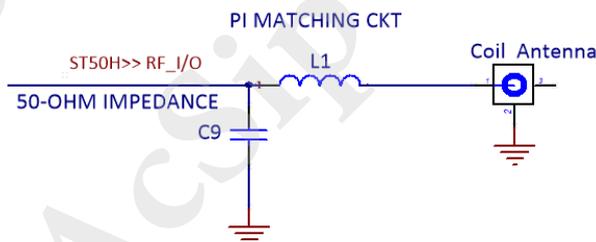
- The values of a and b will affect each other, it is best to control it not to be too wide from the width and gap of the output pad of the module

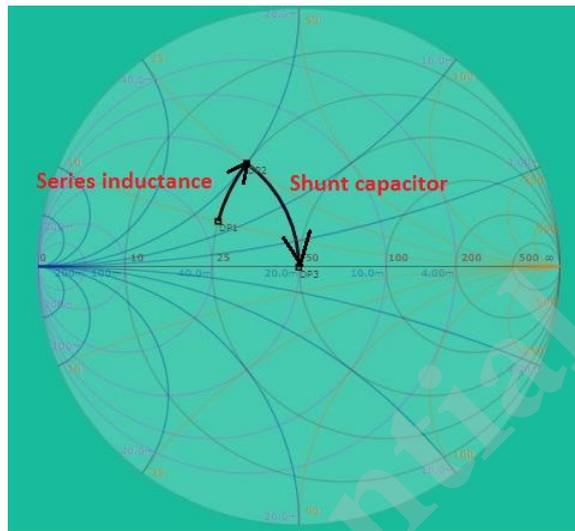


- Suggest customer deploy Pi-matching circuits close to Lora antenna
  - ◆ For 50 ohm matching Antenna application :  
Connect 100 pF at the RF-trace as the flowing reference design



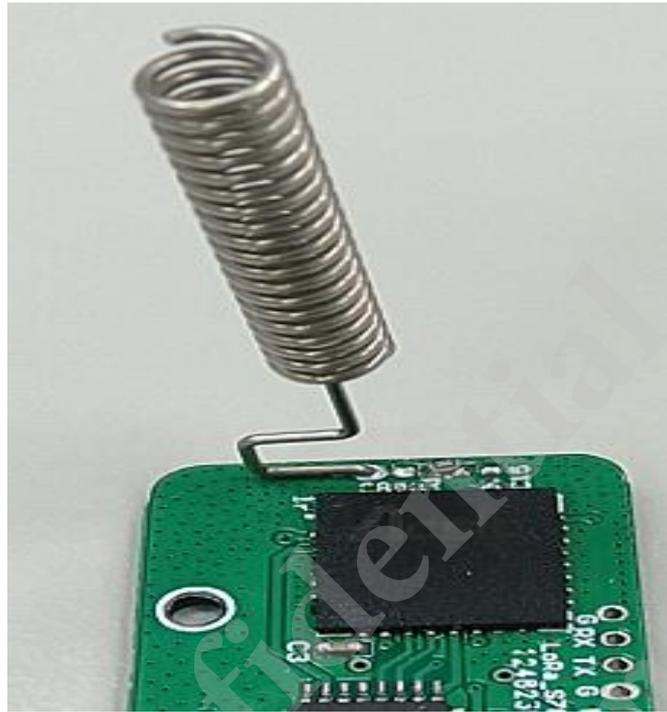
- ◆ If you choose a metal coil antenna, the impedance will be lower (<50 ohms) and it is inductive. Its R+jL is easier to fall on the upper left of the Smith Chart, so series inductance and parallel capacitance are the chosen matching method, but Sometimes for bandwidth, multi-level matching is also used





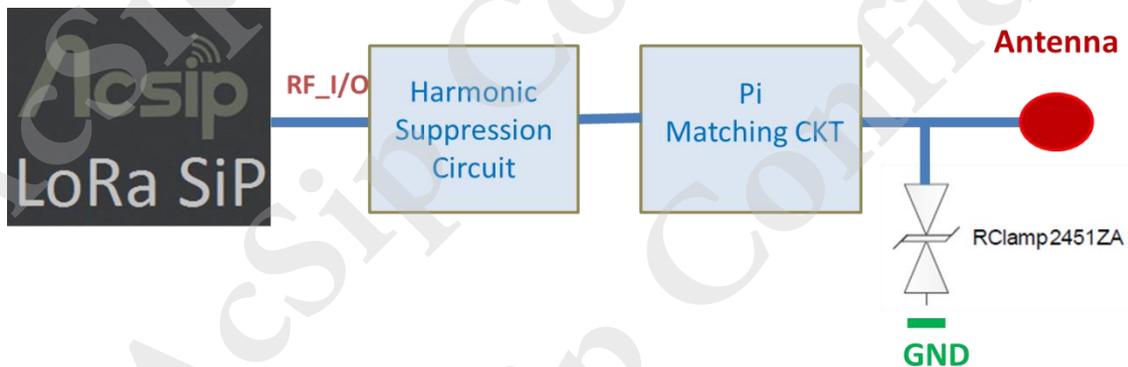
- The Following figures are coil application for Accsip SiP:





### 3.4. ESD Protection

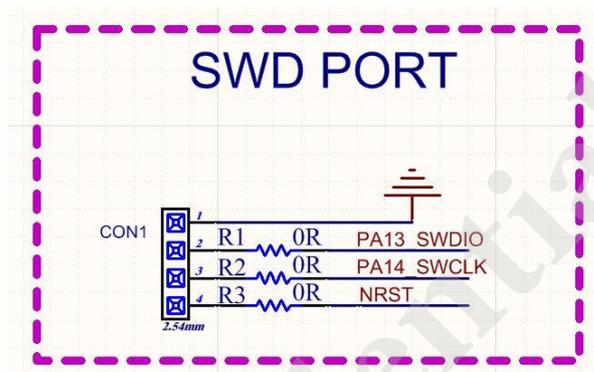
If used in a harsh ESD environment, the following example is reference design for ESD Protection, the recommended part is: Semtech@Rclamp2451z (1-Line, 24 V)



## 3.5. Other Schematic

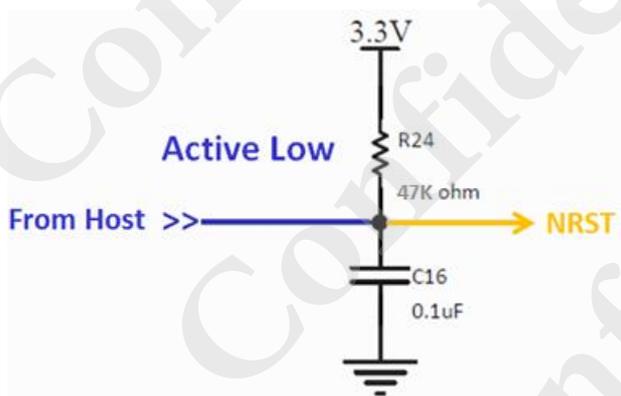
- **ST-LINK SWD Port :**

User needs to connect this three SWDIO , SWCLK & NRST pins with ST-LINK/V2, V3 unit.



- **NRST :**

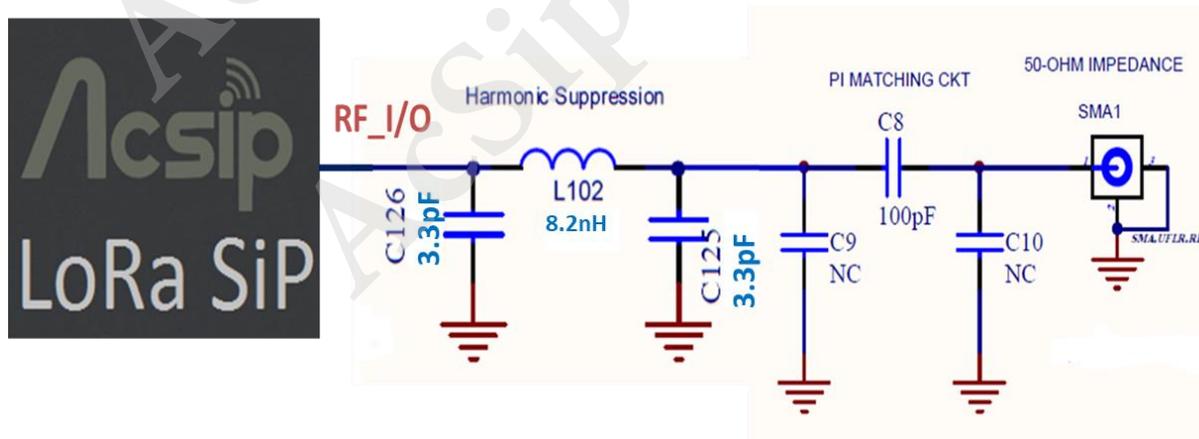
System Reset, Active Low, Please place R24/C16 close to ST50H module.



- **Harmonic suppression**

Whether a harmonic suppression circuit is needed, depends on the EMI test result.

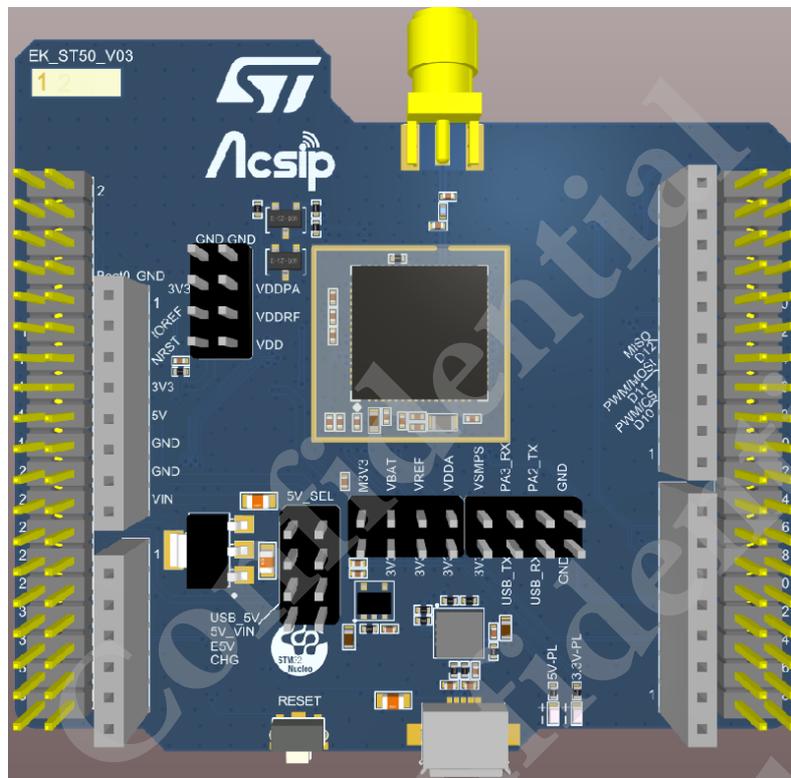
Default value is L102=8.2nH Murata LQW15AN, C125=3.3pF, C126=3.3pF.



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## 3.6. Shielding Cover

Shielding Cover design is recommended for EMI suppression.



## 4. Other Information

- Do not put any signal trace or power trace on system PCB top layer under ST50H module.
- Discuss with AcSiP engineer after schematic and layout finished.
- For Additional information, please contact the following:

AcSiP Technology Corp.

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FAX : +886-2-86859577

Contact : [sales@acsip.com.tw](mailto:sales@acsip.com.tw)

Website : <http://www.acsip.com.tw/>